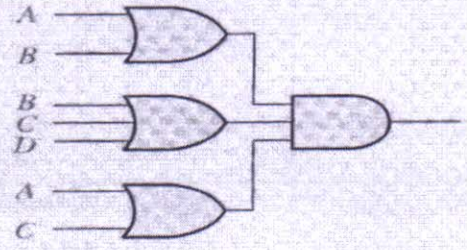
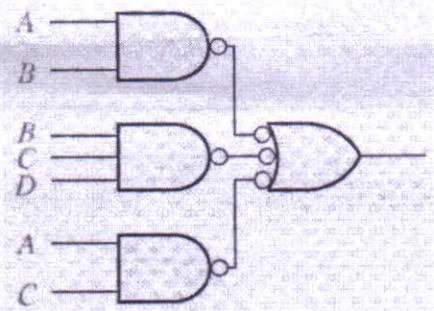
U117-104 A (RE-FFFF)

DECEMBER 2017 / ~~ENDSEM~~ RE EXAM

F. Y. B. TECH. (COMMON) (SEMESTER - I)

COURSE NAME: Basic Electronics Engineering

(2017 PATTERN)

Q.NO	Sub Q.NO	Marking Scheme	Marks	Difficulty Level	Cognitive level	CO Mapped
Q1	a)	Construction of NOT gate using NAND gate:2M Construction of OR gate using NAND gate:2M Construction of AND gate using NAND gate:2M	[6]	M	Comprehension	CO4
	b)	S-R flip flop block diagram :2M Explanation of S-R flip flop working:2M S-R flip flop truthtable:2M	[6]	M	Comprehension	CO4
	c)	 $= AB + BCD + AC$: 2M  $= AB + BCD + AC$: 2M	[4]	L	Comprehension	CO4
		OR				

Q2	a)	Block diagram of full Adder using two half adders: 2M Working and Proper simplified expression for sum and carry: 4M	[6]	M	Comprehension	CO4
	b)	Convert binary number 111010.101 to decimal number: 58.625: 3M Convert decimal number 45.32 to binary number: 101101.01010010: 3M	[6]	H	Comprehension /Application	CO4
	c)	Definition and symbol of NAND and NOR gate: 2M Truth table of NAND and NOR gate: 2M	[4]	L	Knowledge	CO4
Q3	a)	LVDT circuit diagram: 1M Working of LVDT:3M State any two advantages and disadvantages of LVDT: 2M	[6]	M	Knowledge	CO5
	b)	Construction diagram of strain gauge: 2M Explanation of working principle :2M	[4]	L	Knowledge	CO5
	c)	Stating types of pressure transducer: 2M Construction diagram of any two pressure transducer:2M	[4]	L	Knowledge	CO5
		OR				
Q4	a)	Block diagram of basic instrumentation system: 3M Explanation of the block diagram of basic instrumentation system: 3M	[6]	M	Knowledge and Comprehension	CO5

	b)	Explanation of ultrasonic flow meter with diagram:4M	[4]	L	Knowledge	CO5
	c)	Transducer explanation: 2M Classification based on its output (input) quantity measured: 2M	[4]	L	Comprehension	CO5

Q.5

1.	When voltage applied to a diode is more than PIV, it is likely to result in a) More distortion on output side b) Poor regulation c) Conduction in both direction d) Breakdown at the junction. Ans : **d**	[1]
2.	If the ac supply is 50 Hz, what will be the ripple frequency out of the full-wave rectifier? a) 50 Hz b) 60 Hz c) 120 Hz d)100 Hz Ans : **d**	[1]
3.	In what state is a silicon diode if the voltage drop across it is about 0.7 V? a) No bias b) Reverse bias c) Forward bias d) Zener region Ans : **c**	[1]
4.	The no load output voltage of full wave rectifier is a) 0.318 V_{peak} b) 2 V_{peak} c) 0.636 V_{peak} d) 0.5 V_{peak} Ans : **c**	[1]
5.	Which of the following, when added as an impurity, into the silicon, produces n-type semi-conductor a) Aluminium b) Phosphorous c) Magnesium d) both 'b' and 'c' Ans : **b**	[1]
6.	A current ratio of I_C/I_E is usually less than one and is called: a) beta b) alpha c) theta d) omega Ans : **b**	[1]

7.	In which region are both the collector-base and base-emitter junctions forward-biased? a) Saturation b) Cutoff c) Active d)All of the above Ans : **a**	[1]
8.	In the active region for a CE transistor configuration, the collector-base junction is _____-biased, the base-emitter is _____-biased. a) reverse, forward b) forward, reverse c) forward, forward d) reverse, reverse Ans : **a**	[1]
9.	For what kind of amplifications , the active region of the common-emitter configuration be used? a)Voltage b)Current c)Power d) All of the above Ans : **d**	[1]
10.	Three different Q points are shown on a dc load line. The upper Q point represents the: a) minimum current gain b) intermediate current gain c) cutoff point d) maximum current gain Ans : **d**	[1]
11.	Which of the following devices does not have a cathode terminal? a) SCR b) PN Junction Diode c)Triac d) Zener diode Ans : **c**	[1]

12.	It is the insulating layer of _____ in the MOSFET construction that accounts for the very desirable high input impedance of the device. a) SiO b) GaAs c) SiO_2 d) HCl Ans : **c**	[1]
13.	This symbol is of _____  a) SCS b) SCR c) GTO d)DIAC Ans : **b**	[1]
14.	The triac is a) a four-terminal device b) like a bidirectional SCR c) not a thyristor d) answers (a) and (b) Ans : **b**	[1]
15.	Which of the following applies to MOSFETs? a) All of the below b) Desirable high input impedance c) Uses metal for the gate, drain, and source connections d) No direct electrical connection between the gate terminal and the channel Ans : **a**	[1]
16.	When an op-amp is operated in the single-ended differential mode a) one input is grounded and a signal is applied to the other b) the output is grounded c) both inputs are connected together d) the output is not inverted Ans : **a**	[1]
17.	A differential amplifier	[1]

	a) is intermediate stage of OPAMP b) has one input and one output c) has no outputs d) is first stage of OPAMP Ans : **d**	
18.	The use of negative feedback a) reduces the voltage gain of an op-amp b) makes the op-amp oscillate c) makes linear operation possible d) answers (a) and (c) Ans : **d**	[1]
19.	Negative feedback a) increases the input and output impedances b) decreases the output impedance and the bandwidth c) increases the input impedance and the bandwidth d) does not affect impedances or bandwidth Ans : **c**	[1]
20.	The maximum slew rate of IC 741 is a) 0.1 V/ns b) 0.8 V/ns c) 0.5 V/ns d) 1 V/ns Ans : **c**	[1]