Total No. of Questions – [05] Total No. of Printed Pages [2]

G.R. No.	

Paper Code - U127-104A (ESE)

MAY 2018 / ENDSEM

F. Y. B. TECH. (COMMON) (SEMESTER - II)

COURSE NAME: Basic Electronics Engineering

ET10174A **(2017 PATTERN)**

Time: [**2 Hours**] [Max. Marks: **50**]

(*) Instructions to candidates:

1) **Answer Q.1 OR Q.2, Q.3 OR Q.4 and Q.5**
2) **Figures to the right indicate full marks.**
3) **Use of scientific calculator is allowed.**
4) **Use suitable data wherever required.**

Q.1 **a)** State and prove Demorgan's theorems, Draw the logical diagrams. **[6]**

b) What is Multiplexer? Draw 4:1 multiplexer and develop logical expression for the output. **[6]**

c) Explain the reasons due to which digital technology is preferred over analog technology. **[4]**

OR

Q.2 **a)** Explain commutative law, associative law and distributive law using logic expressions. **[6]**

b) Convert binary number 110110.1011 to decimal number and convert decimal number 82.625 to binary number. **[6]**

c) Using basic logic gates implement the following logical expressions **[4]**

1) $X = A\bar{B} + AB$

2) $X = \overline{ABC} + B(EF + \bar{G})$

Q.3 **a)** What is RTD? Explain its construction and working principle. Draw the circuit diagram for measurement of temperature using RTD. **[6]**

b) What is strain gauge? How it is used to measure weight? **[4]**

c) Explain any four characteristics of transducer. **[4]**

OR

Q.4 a) Draw the construction diagram of thermister and explain the working principle of it. **[6]**

b) Explain working of ultrasonic flow meter. **[4]**

c) What are passive transducers? List the categories in which they are classified. **[4]**

Q.5 Attempt following multiple choice questions:[2x10=20 marks]

1. Three LED's are connected in series along with limiting resistance. It is supplied with 12 V DC ,current flowing through LED is 20mA and drop across each LED is 2.5V, the value of limiting resistance will be **[2]**
   a) 200 Ω b) 250 Ω c) 225 Ω d) 300 Ω

2. The voltage across Zener diode remains constant when operated **[2]**
   a) Below Iz_{min} b) between Iz_{min} and Iz_{max} c) in forward biased d) None of the above

3. A properly biased single stage transistor amplifier has gain of 56 and dynamic emitter resistance of 10 Ω ,the collector resistance will be **[2]**
   a) 56 Ohm b) 560 Ohm c) 5.6 K Ohm d) 10 Mho

4. V_{CE} approximately equals _____ when a transistor is in saturation state. **[2]**
   a) V_B b) V_{CC} c) 0.2 V d) 10V

5. Ideal op-amp has -------- CMRR and ---------input offset voltage **[2]**
   a) infinity, zero b) infinity, infinity c) zero, zero d) zero, infinity

6. In inverting amplifier R_F=50KΩ and R_1=2KΩ then the close loop gain of amplifier is **[2]**
   a) -25 b) 26 c) -52 d) 100

7. In Non inverting comparator, the output of comparator will be at --------, when it's input voltage is greater than reference voltage i.e V_{ref} =1V. **[2]**
   a) negative saturation b) positive saturation c) zero volt d) 1 volt

8. For SCR with firing angle of α=0, the DC voltage at the output of full wave controlled rectifier is **[2]**
   a) Vm/π b) 2Vm/π c) Vm/2π d) 0

9. For n channel E-MOSFET, if V_{GS}=5V, Vth=1V and K=6.17mA/V^2 the drain current is **[2]**
   a) 95mA b) 90.18mA c) 98.7mA d) 101.24mA

10. The output of a particular op-amp increases 10V in 16μs. The slew rate is **[2]**
    a) 62.5V/μs b) 0.625V/μs c) 1.5V/ μs d) none of these