MAY 2018 / ENDSEM

F. Y. B. TECH. (COMMON) (SEMESTER - II)

COURSE NAME: Basic Electronics Engineering

(2017 PATTERN)

Paper Code - U127-104A (ESE)

Q.NO	Sub Q.NO	Marking Scheme	Marks	Difficulty Level	Cognitive level	CO Mapped
Q1	a)	State Demorgan's theorems,: 2M Prove Demorgan's theorems,: 2M Draw the logical diagrams.: 2M	[6]	L	Knowledge/ Comprehension	CO4
	b)	What is Multiplexer:2M Draw 4:1 multiplexer:2M Develop logical expression for the output:2M	[6]	M	Comprehension	CO4
	c)	Explanation for the reasons of digital technology is preferred over analog technology: 4M	[4]	M	Comprehension	CO4
OR						
Q2	a)	Commutative law using logic expressions:2M Associative law using logic expressions:2M Distributive law using logic expressions:2M	[6]	L	Knowledge	CO4
	b)	Convert binary number 110110.1011 to decimal number 54.6875 : 3M Convert decimal number 82.625 to binary number is 1010010.101:3M	[6]	H	Comprehension /Application	CO4
	c)	Using basic logic gates implement the following logical expressions 1) $X = A\bar{B} + AB$ 2M 2) $X = \overline{ABC} + B(EF + \bar{G})$:M	[4]	M	Comprehension	CO4
Q3	a)	What is RTD:1M Construction and working principle: 3M.	[6]	M	Knowledge	CO5

		Circuit diagram for measurement of temperature using RTD:2M				
	b)	What is strain gauge: 1M How it is used to measure weight:3M	[4]	L	Knowledge	CO5
	c)	Explanation of four characteristics of transducer: 4M	[4]	L	Knowledge	CO5
		OR				
Q4	a)	Construction diagram of thermistor:2M Explain the working principle of it:4M	[6]	M	Knowledge and Comprehension	CO5
	b)	Explanation of working of ultrasonic flow meter: 4M	[4]	L	Knowledge	CO5
	c)	What are passive transducers :2M List the categories in which they are classified: 2M	[4]	L	Comprehension	CO5

Q.5

1.	Three LED's are connected in series along with limiting resistance. It is supplied with 12 V DC ,current flowing through LED is 20mA and drop across each LED is 2.5V, the value of limiting resistance will be a) 200 Ω b) 250 Ω c) 225 Ω d) 300 Ω Ans: c	[2]
2.	The voltage across Zener diode remains constant when operated a) Below Iz_{min} b) between Iz_{min} and Iz_{max} c) in forward biased d) None of the above Ans: b	[2]
3.	A properly biased single stage transistor amplifier has gain of 56 and dynamic emitter resistance of 10 Ω ,the collector resistance will be a) 56 Ohm b) 560 Ohm c) 5.6 K Ohm d) 10 Mho. Ans: b	[2]
4.	V_{CE} approximately equals _____ when a transistor is in saturation state. V_B b) V_{CC} c) 0.2 V d) 10V Ans: c	[2]

5.	Ideal op-amp has -------- CMRR and ---------input offset voltage a) infinity, zero b) infinity, infinity c) zero, zero d) zero, infinity Ans: a	[2]
6.	In inverting amplifier R_F=50KΩ and R_1=2KΩ then the close loop gain of amplifier is a) -25 b) 26 c) -52 d) 100 Ans: a	[2]
7.	In Non inverting comparator, the output of comparator will be at -------- when it's input voltage is greater than reference voltage i.e V_{ref} =1V. a) negative saturation b) positive saturation c) zero volt d) 1 volt Ans: b	[2]
8.	For SCR with firing angle of α=0, the DC voltage at the output of full wave controlled rectifier is a) Vm/π b) $2Vm/\pi$ c) $Vm/2\pi$ d) 0 Ans: b	[2]
9.	For n channel E-MOSFET, if V_{GS}=5V, Vth=1V and K=6.17mA/V^2 the drain current is a) 95mA b) 90.18mA c) 98.7mA d) 101.24mA Ans: b	[2]
10.	The output of a particular op-amp increases 10V in 16μs. The slew rate is a) 62.5V/μs b) 0.625V/μs c) 1.5V/ μs d) none of these Ans: b	[2]