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S.I	E. (C	computer Engg.) (First Semester) EXAMINATION, 2017	
		MICROPROCESSOR ARCHITECTURE	
		(2012 PATTERN)	
Time	e : T	Two Hours Maximum Marks : 5	0
N.B.	:	(i) Attempt Q. No. 1 or Q. No. 2, Q. No. 3 or Q. No. 4	1,
		Q. No. 5 or Q. No. 6, Q. No. 7 or Q. No. 8.	ĺ
	((ii) Neat diagrams must be drawn wherever necessary.	
		iii) Figures to the right indicate full marks.	
	^	(iv) Assume suitable data, if necessary.	
	1	10) Assume suitable data, il necessary.	
1	(~)	Evaloin the test mediators with their formet	rσ
1.	(a)	Explain the test registers with their format. [3]	_
	(<i>b</i>)	Differentiate between Min mode and Max mode of 808	
		processor [4	_
	(c)	Explain the following pins of 8086:	i [č
		(i) INTA#	3
		(ii) HLDA	4
		(iii) DT/R#	
		Or	
2.	(a)	Specify size and function of IDTR.	3]
	(<i>b</i>)	Explain the hardware interrupt pins of 80386 processor. [4]	<u>[</u>]
	(c)	Draw and explain the functional pin diagram of 80386 D	X
		processor.	3]
		Cy Si	

- 3. (a) Draw and explain non-pipelined write cycle of 80386 DX. [5]
 - (b) Explain HOLD/HLDA signal.

[4]

(c)	Explain with example difference between SUB and SBB
	instruction. [3]
	Or Or
(a)	Explain the following instructions: [5]
	(i) XOR
	(ii) TEST
	(iii) WAIT
	(iv) STD
X.	(v) SHLD.
(<i>b</i>)	What do you mean by assembler directives? Explain any three
	assembler directives used in 80386 programming. [4]
(c)	Explain the assembly language programming steps. [3]
(a)	Explain in detail multiprocessor architecture. [6]
(<i>b</i>)	Give the parallel programming with diagram. [4]
(c)	Briefly explain hybrid multicore architecture. [3]
(0)	Or Or
(a)	Draw and explain the block diagram of 64-bit architecture. [6]
<i>(b)</i>	Write a short note on multicore application design and
	implementation. [4]
(c)	Explain front side and black side bus. [3]
	(a) (b) (c) (a) (b) (c) (a) (b) (c)

7.	(a)	Explain the IA-32 basic execution environment.	[5]
	<i>(b)</i>	State the two sub-modes of IA-32e mode.	[4]
	(c)	What are the advantages of hyper threading technology?	[3]
		Or	
8.	(a)	Explain in detail microarchitecture code name Nehalem.	[5]
	<i>(b)</i>	List the features of SSE2 extensions in Pentium 4 and In	ntel
		Xeon processor.	[4]
	(c)	Explain the features of Virtualization Technology.	[3]
		And the reaction of virtualization regularity. And the reaction regularity.	