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S.E.(I.T.) (First Semester) EXAMINATION, 2017
Digital Electronics and Logic Design
(2012 PATTERN)

Time : Two Hours　　　　　　　　　　　　**Maximum Marks : 50**

N.B. :— (i)　Neat diagrams must be drawn wherever necessary.

(ii)　Figures to the right side indicate full marks.

(iii)　Use of calculator is not allowed.

(iv)　Assume suitable data if necessary.

1. (a)　Convert the decimal number 82.67 and 121.25 to its binary, hexadecimal and octal equivalents.　　　　[6]

   (b)　Explain any *three* IC characteristics and state their values for standard TTL and CMOS family.　　　　[6]

   (1)　Propagation Delay

   (2)　Noise Margin

   (3)　Fan-in and Fan-out

   (4)　Figure of Merit

Or

2. (a)　Perform the following binary arithmetic's using 2's complement method :

   (i)　$(-20)_{10}$ + $(25)_{10}$

   (ii)　$(+20)_{10}$ + $(-25)_{10}$

   (iii)　$(-20)_{10}$ + $(-25)_{10}$　　　　　[6]

   (b)　What do you mean by Half Adder and Full Adder ? How will you implement full adder using Half Adder ? Explain with circuit diagram.　　　　[6]

P.T.O.

3. (*a*) What do you mean by Master Slave JK Flip-Flop ? Explain the working of this Flip-Flop to eliminate race around condition. [6]

(*b*) Draw 4-bit ring and twisted ring counter. Draw state diagram for both assuming initial state as 1000. [7]

Or

4. (*a*) Convert JK Flip-Flop to T Flip-Flop and D Flip-Flop. Show all the design steps. [6]

(*b*) Draw an ASM chart and use multiplexer controller method to design 2-bit up/down counter having mode control input M such that when M = 1 : Up Counting & when M = 0 : Down Counting. The circuit should generate output 1 whenever count become minimum or maximum. [7]

5. (*a*) Draw the basic structure of FPGA. Explain its feature in brief. [6]

(*b*) Implement the following function using Programmable Logic Device.

$$F_1 = \sum m \ (0, \ 3, \ 4, \ 7)$$
$$F_2 = \sum m \ (1, \ 2, \ 5, \ 7)$$ [6]

Or

6. (*a*) Write any *two* comparisons between PROM, PLA and PAL. [6]

(*b*) Draw a PLA circuit to implement the logic function. [6]

$$F_1 = X_1X_2 + X_1X_3' + X_1'X_2'X_3'$$
$$F_2 = X_1X_2 + X_1'X_2'X_3 + X_1X_3$$

7. (*a*) Write VHDL description of D Flip-Flop with Asynchronous reset. [6]

(*b*) Describe different modeling styles of VHDL with suitable example. [7]

Or

8. (*a*) With the help of suitable example explain the data object :

(1) Signal

(2) Variable

(3) Constant [6]

(*b*) Write entity and architecture declaration of a 4 bit adder. [7]