

May 2017

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Seat No.	
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[5152]-562

S.E. (Computer Engineering) (I Sem.) EXAMINATION, 2017

DIGITAL ELECTRONICS AND LOGIC DESIGN

(2015 PATTERN)

Time : Two Hours

Maximum Marks : 50

- N.B. :—** (i) Attempt Q. No. 1 or Q. No. 2, Q. No. 3 or Q. No. 4,
Q. No. 5 or Q. No. 6, Q. No. 7 or Q. No. 8.
(ii) Neat diagram must be drawn wherever necessary.
(iii) Assume suitable data if necessary.

1. (a) Implement the expression using a 8 : 1 multiplexer [4]
$$f(a, b, c, d) = \sum m(0, 2, 3, 6, 8, 9, 12, 14).$$

(b) What is the difference between combinational and sequential circuits ? [2]
(c) Simplify the following logic function using the Quine-McCluskey minimization technique : [6]
$$Y(A, B, C, D) = \sum m(0, 1, 3, 7, 8, 9, 11, 15).$$

Or

2. (a) Explain in detail look ahead carry generator [6]
(b) Design Mod-24 counter using 7490 [2]
(c) Design a sequence detector using MS J-K flip-flop sequence is 1101. [4]

P.T.O.

3. (a) Draw ASM chart for 2-bit UP counter using multiplexer controller method. [8]
- (b) List any *two* modeling style of VHDL [2]
- (c) Compare concurrent and sequential statement in VHDL [2]

Or

4. (a) Design 4 input and 6 output combinational circuit using PLA. The input variables are A, B, C and D : [6]

$$Y1 = \Sigma m(0, 3, 5, 6, 9, 10, 12, 15)$$

$$Y2 = \Sigma m(0, 1, 2, 3, 11, 12, 14, 15)$$

$$Y3 = \Sigma m(0, 4, 8, 12)$$

$$Y4 = \Sigma m(0, 2, 3, 5, 7, 8, 12, 13)$$

$$Y5 = \Sigma m(0, 1, 3, 4, 5, 6, 11, 13, 14, 15)$$

$$Y5 = \Sigma m(1, 2, 6, 8, 15).$$
- (b) Draw block diagram of PLA device and explain. [6]
5. (a) Explain characteristics of digital ICs (any *four*). [4]
- (b) Explain operation of TTL NAND gate. [6]
- (c) Explain TTL open collector [3]

Or

6. (a) What is addressing mode ? Identify and justify addressing modes of the following 8051 instructions : [6]
 - (i) MOVX A, @DPTR
 - (ii) MOVC A, @ A+PC
 - (iii) ADD A, #10
 - (iv) MOV DPTR, #2550.
- (b) What is microcontroller ? Distinguish between microcontroller and microprocessor. [7]

7. (a) Explain CMOS inverter. [4]
(b) Why wired logic is not possible in CMOS operation. [4]
(c) Explain tristate logic. [5]

Or

8. (a) Explain the physical structure and significances of all I/O ports of 8051 microcontroller. [7]
(b) Give significance of the following pins in 8051 : [6]
(i) PSEN#
(ii) EA#/VPP
(iii) ALE
(iv) TxD
(v) INT0#
(vi) RST.