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**[5152]-573**

**S.E. (Information Technology) (First Semester)**

**EXAMINATION, 2017**

**DIGITAL ELECTRONICS AND LOGIC DESIGN**

**(2015 Course)**

**Time : Two Hours**

**Maximum Marks : 50**

**N.B. :—** (i) Answer Question 1 or 2, 3 or 4, 5 or 6 and 7 or 8.

(ii) Neat diagrams must be drawn wherever necessary.

(iii) Figures to the right indicate full marks.

(iv) Assume suitable data, if necessary.

1. (a) Explain any *three* characteristics of Digital ICs. [6]

(b) Implement the following Boolean function using single 8:1 multiplexer : [6]

$$F(A, B, C, D) = \Sigma m(1, 4, 6, 9, 13)$$

Or

2. (a) Do the following [6]

(i)  $(7F)_{16} - (5C)_{16}$  using 2's complement method

(ii)  $(735.25)_{10} = (?)_{16}$

(iii)  $(101011.111011)_2 = (?)_8 (?)_{16}$

(b) Simplify the following Boolean function using Quine MC-Clusky Technique  $F(A, B, C, D) = \Sigma(0, 1, 3, 7, 8, 9, 11, 15)$ . [6]

3. (a) Design and draw logic diagram of mod 45 counter using IC 7490 [6]

(b) Design sequence generator to generate the sequence 1011 using shift register IC 74194. [6]

P.T.O.

*Or*

4. (a) Explain with a neat diagram Ring Counter. [6]  
(b) Design flip-flop conversion logic to convert JK flip-flop to T flip-flop. [6]
5. (a) Draw the ASM chart for 2-bit binary Up/ Down counter with control input M such that if M=0 counter counts in Up direction and if M=1 Counter counts in Down Direction. Design the same using MUX Controller Method using D flip-flops. [7]  
(b) Explain architecture of CPLD with the help of suitable diagram. [6]

*Or*

6. (a) Design Full Adder using PLA [7]  
(b) Compare CPLD and FPGA [6]
7. (a) Explain VHDL modeling styles with example. [7]  
(b) Write VHDL program for 3:8 decoder. [6]

*Or*

8. (a) What is VHDL ? Write features of VHDL. Explain the structure of VHDL module. Define entity and architecture for 2 input OR gate. [7]  
(b) Explain the difference between concurrent and sequential statements with an example. [6]