Total No. of Questions : 12]

SEAT No. :

P2449

[Total No. of Pages :3

[5153]-83
T.E. (Computer Engineering)
MICROPROCESSORS AND MICROCONTROLLERS
(2008 Course) (Semester - I) (310243)

Time : 3 Hours] *[Max. Marks :100*

Instructions to the candidates:

1) ***Answer Question No. 1 OR 2, 3 OR 4, and 5 OR 6 from Section I and Q. No. 7 OR 8, 9 OR 10 and 11 OR 12 from Section II.***
2) ***Answers to the two Sections must be written in separate answer books.***
3) ***Neat diagrams must be drawn whenever necessary.***
4) ***Figures to the right indicate full marks.***
5) ***Assume suitable data, if necessary.***

SECTION - I

Q1) a) Compare 80386, 80486, and the Pentium based on architecture. **[6]**

b) Explain Floating Point Unit of the Pentium? **[6]**

c) What is the function of each of the following pins? **[6]**

i) BRDY #

ii) ADS #

iii) BE0 # - BE 7 #

OR

Q2) a) Describe cache organization of the Pentium. **[6]**

b) Which features makes the Pentium, a superscalar processor? Explain in detail. **[6]**

c) What is Branch Prediction in the Pentium? Explain with diagram. **[6]**

Q3) a) Explain addressing modes of the Pentium. **[8]**

b) What is the purpose of control registers? Explain significance of CR0 in working of cache and paging unit. **[8]**

OR

P.T.O.

Q4) a) With the help of neat diagram, explain non-pipelined read bus cycle of the Pentium. **[6]**

b) List and explain protected mode registers of the Pentium. **[6]**

c) Describe any two instructions. **[4]**

i) XADD

ii) BTC

iii) SWAPB

Q5) a) How linear address is translated to physical address in the Pentium. Draw the required data structures. **[8]**

b) Describe call gate mechanism in details. Draw the related descriptor formats. **[8]**

OR

Q6) a) How logical address is translated to linear address in the Pentium. Draw the required data structures. **[8]**

b) How pages can be protected in the Pentium? Give details. **[8]**

SECTION - II

Q7) a) What is I/O permission bit map? When it is referred? **[6]**

b) Explain task switch operation through task gate. **[6]**

c) Write any six difference between 8086 and virtual 86 mode. **[6]**

OR

Q8) a) Explain IDT in Pentium in details. How interrupt handling in protected mode is dependent on contents of IDT? **[6]**

b) Explain steps in entering Virtual mode. **[6]**

c) Explain nested task in the Pentium. **[6]**

Q9) a) Draw and Explain internal RAM organization of 8051. **[12]**

b) Explain the function of following pins. **[4]**

i) TI

ii) T0

OR

Q10)a) Explain addressing modes of 8051 microcontroller. Explain with suitable example. **[8]**

b) Explain following 8051 instructions. **[8]**

i) MOVC

ii) MOVX

iii) SETB

iv) RETI

Q11)a) Write features of 8096 microcontroller. **[4]**

b) Explain IE & IP registers of 8051 microcontroller. **[8]**

c) Explain any two modes of timer operation in 8051. **[4]**

OR

Q12)a) How many interrupt sources are there in 8051? List them & explain interrupt handling mechanism in 8051. **[8]**

b) Describe serial port on 8051 with the help of SCON. **[8]**