Total No. of Questions : 12]

SEAT No. :

P2002

[Total No. of Pages : 3

[5254] - 173
B.E. (Computer) (Semester - II)
ADVANCED COMPUTER ARCHITECTURE
(2008 Pattern)

Time : 3 Hours] *[Max. Marks : 100*

Instructions to the candidates :

1) ***Answer any three questions from each section.***
2) ***Answers to these sections should be written in separate books.***
3) ***Neat diagrams must be drawn wherever necessary.***
4) ***Figures to the right indicate full marks.***
5) ***Assume suitable data, if necessary.***

SECTION - I

Q1) a) Mention the two categories of parallel Computers and explain the same with architecture. **[10]**

b) Define and Explain following terms : **[8]**

i) Grain Packing

ii) Coarse Grain

iii) Fine Grain

OR

Q2) a) What is parallel processing? State the following terms with respect to parallelism : **[10]**

i) Thread Level Parallelism (TLP)

ii) Software Parallelism

iii) Instruction Level Parallelism (ILP)

iv) Speedup

b) Explain how two architectural design approaches namely Super scalar and super pipeline improves pipelining performance with respect to following parameters : **[8]**

i) Machine pipeline cycle

ii) Instruction issue rate

iii) Instruction issue latency

P.T.O.

Q3) a) For a linear pipeline processor, considering a single k-stage pipeline executing N instructions, obtain the various performance parameters. **[8]**

b) What is internal forwarding? Explain the various internal forwarding techniques. **[8]**

OR

Q4) a) Compare between arithmetic and instruction pipeline. Design a 6-bit multiplier using CSA tree. How it can be viewed as k-stage pipeline? **[8]**

b) Define static and dynamic pipeline. What is the use of Reservation Table? Explain the control strategy implemented for job sequencing problem. **[8]**

Q5) a) Describe following terms with respect to vector processors : **[8]**

i) Vector Stride

ii) Vector Chaining

iii) Vector Mask Register

iv) Vector Mask Control

b) Consider Mesh network as an interconnection network for array processors. Discuss in detail the parallel Algorithm for Matrix Multiplication. Obtain the time Complexity for the same. **[8]**

OR

Q6) a) How a 3-cube Network can be viewed as Multistage Network? **[8]**

b) Discuss any two Vector Optimization functions implemented in Vectorizing Compiler. **[8]**

SECTION - II

Q7) a) What is an Interprocess synchronization? How it is implemented at system level? Discuss the working of compare and swap instruction for the same. **[10]**

b) What is Interprocess synchronization and communication? Discuss the hardware support provided by machine architecture by means of suitable instructions for the same. **[8]**

OR

Q8) a) What is chip multiprocessing? With functional block diagram explain the architecture of IBM POWER4/POWER5 processor. **[10]**

b) List different dynamic priority arbitration algorithms used in bus based multi-processor systems and discuss any two such algorithms in brief. **[8]**

Q9) a) What Basic Concept of Multithreading? Explain Multithreaded Architectures and its Computational Model for Parallel Processing System. **[8]**

b) Compare efficiency of multithreading implemented in Superscalar architecture with respect to coarse grained, fine grained and simultaneous multithreading. **[8]**

OR

Q10) Write short note on any two : **[16]**

a) Context Switching Policies of Multithreaded Architectures

b) P threads

c) Semaphore for multiprocessing

Q11) a) Explain following communication functions used in MPI : **[8]**

i) MPI_Scatter()

ii) MPI_Gather()

iii) MPI_Bcast

iv) MPI_Allgather

b) With standard functions discuss how message passing is facilitated in PVM. **[8]**

OR

Q12) a) With standard constructs discuss the important features of CCC parallel programming language. **[8]**

b) Compare between synchronous and Asynchronous parallel algorithms for multiprocessor systems and discuss standard primitives used. **[8]**

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