Tota	l No.	of Questions : 12] SEAT No. :						
P19	79	[Total No. of Pages : 3						
		[5254]-88						
	B.E. (Electronics Engineering) (Semester -I)							
ADVANCED COMPUTER ARCHITECTURE (Elective -II)								
		(2008 Pattern)						
		Iours] [Max. Marks: 100						
Instr	ructio 1)	Answer anythree questions from each section						
		Answer any three questions from each section.						
	<i>2) 3)</i>	Answer of the two sections should be written in separate answer books. Neat diagrams must be drawn wherever necessary.						
	<i>4</i>)	Assume suitable data, if necessary.						
	1)	11ssume sumable data, if necessary.						
		<u>SECTION - I</u>						
Q1)	a)	Explain Handler's classification and Feng's classification for parallel computer architectures. [12]						
	b)	Explain instruction level parallelisim. [6]						
OR								
Q2)	a)	Discuss any two applications of parallel processing in detail. [12]						
	b)	Explain the Von-Neuman computer architecture and its limitations. [6]						
	-							
Q3)	a)	Explain the loop unrolling techniques & its use. [8]						

Compare superscalar and VLIW processor.

b)

Q4) a) Explain the internal forwarding Techniques. [8]

OR

b) Explain with suitable examples, the various types of hazards in a pipeline processor. How these hazards can be resolved? [8]

[8]

<i>Q5</i>)	a)	What are vector processors? Discuss two different architectural configurations of vector processor. [12]						
	b)	Explain pipeline chaining. [4]						
OR								
Q6)	a)	State the characteristics of CRAY -I computer system. Draw and explain the computation section of CRAY -I vector processor. [12]						
	b)	Explain any two types of vector instructions. [4]						
		<u>SECTION - II</u>						
<i>Q7</i>)	a)	Explain the algorithm to compute fast fourier transform for SIMD architecture. [10]						
	b) Explain cube interconnection network and hyper cube network.							
		OR						
Q8)	a)	Explain matrix multiplication on SIMD architecture. [10]						
	b)	Describe the following system inter connection architectures: [8]						
		i) Static interconnection						
		ii) Dynamic interconnection						
Q9)	a)	i) State features of IBM power 4 processor. [4]						
		ii) Explain chip multiprocessing. [4]						
	b)	Explain cache coherancy and bus snooping. [8]						

Q10)a)	Exp	plain in detail, the architecture of MPP.	[8]						
b)	Write a note on interprocess communication and synchronization.								
Q11)a)	What is multithreading? Explain following performance measur parameters.								
	i)	Latency (L)							
	ii)	Number of threads (N)							
	iii)	Context switching overhead (C)							
	iv)	Interval between switches (R)							
b)	Write a short note on latency hiding techniques.								
	OR								
<i>Q12</i>)a)	Explain different context switching policies adopted by multith architectures.								
b)	Write short note on-								
	i)	Synchronous message passing							
	ii)	Asynchronous message passing							