Total No. of Questions : 12]

SEAT No. :

P1973

[Total No. of Pages : 3

[5254]-82
B.E. (Electronics Engineering) (Semester -I)
VLSI DESIGN
(2008 Pattern)

Time : 3 Hours] *[Max. Marks : 100*

Instructions to the candidates:

1) ***Answer Q1 or Q2, Q3 or Q4 Q5 or Q6 from Section-I and Q7 or Q8, Q9 or Q10, Q11 or Q12 from Section-II.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right side indicate full marks.***
4) ***Assume Suitable data, if necessary.***

SECTION - I

Q1) a) Explain Body effect and Channel length modulation in detail. **[8]**

b) What are advantages of CMOS and explain CMOS inverter circuit with Voltage transfer curve. **[8]**

OR

Q2) a) Explain Technology scaling with recent developments VLSI. **[8]**

b) Explain Power consumption in CMOS? Derive the expression. **[8]**

Q3) a) Write a short note on 6T cell. **[8]**

b) What is the role of memories in PLDs? Explain in detail. **[8]**

OR

Q4) a) Which are different refresh circuits are available for memories? Explain in detail. **[8]**

b) Compare SRAM and DRAM. **[8]**

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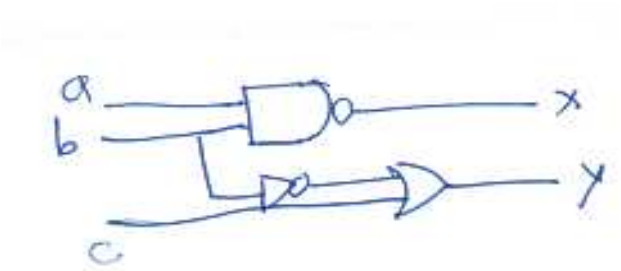
Q5) a) Differentiate between synchronous and asynchronous machines? **[9]**

b) What are function? Explain where it is needed and with how it is implemented in VHDL code with one example. **[9]**

OR

Q6) a) What are the data objects in VHDL programs. **[9]**

b) Write VHDL code for following circuit with structural modeling. **[9]**



SECTION - II

Q7) a) How logic is getting implemented in FPGA? Explain with half adder circuit. **[9]**

b) What is the role of Configurable Logic Block in FPGA? Explain in detail. **[9]**

OR

Q8) a) Draw and explain internal structure of CPLD and enlist important features. **[9]**

b) Compare CPLD with FPGA? **[9]**

Q9) a) Explain different types of faults? **[8]**

b) Explain controllability, predictability, testability in detail. **[8]**

OR

Q10)a) What is partial scan and full scan checks? **[8]**

b) Write short note on Built in self test (BIST) **[8]**

Q11)a) Give different power distribution techniques in detail. **[8]**

b) Explain I/O architecture in brief. **[8]**

OR

Q12)a) What is clock skew? Clock jitter? Explain its importance in chip design. **[8]**

b) Write short note on Power optimization. **[8]**

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