Total No. of Questions—8] [Total No. of Printed Pages—3

Seat No.	

[5252]-163

SE (Computer) (I Sem.) EXAMINATION, 2017

DIGITAL ELECTRONICS AND LOGIC DESIGN

(2012 PATTERN)

Time : Two Hours **Maximum Marks : 50**

N.B. :— (*i*) Solve Q. No. **1** *or* Q. No. **2**, Q. No. **3** *or* Q. No. **4**, Q. No. **5** *or* Q. No. **6** and Q. No. **7** *or* Q. No. **8**.

(*ii*) Neat diagrams must be drawn wherever necessary.

(*iii*) Figures to the right indicate full marks.

(*iv*) Use of Mollier charts, electronic pocket calculator and steam tables are allowed.

(*v*) Assume suitable data, if necessary.

1. (*a*) Minimize the following function using K-map and realize using logic gates : [4]

$F(A, B, C, D) = \Sigma m(1, 5, 7, 13, 15) + d(0, 6, 12, 14)$.

(*b*) Convert the following : [2]

$$(175)_{10} = (?)_8$$

(*c*) List the differences between CMOS and TTL. [6]

Or

2. (*a*) Convert the following numbers into binary numbers : [4]

(*i*) $(37)_8$

(*ii*) $(25.5)_{10}$

(*b*) Explain the standard TTL characteristics in detail. [6]

P.T.O.

(*c*) Represent the following signed number in 2's complement method : [2]

(*i*) +17

(*ii*) –17.

3. (*a*) Explain rules for BCD addition with suitable example and design a single digit BCD adder using IC 7483. [6]

(*b*) Design a MOD-6 synchronous counter using J-K flip-flops. [6]

Or

4. (*a*) Design a sequence generator using J-K flip-flop sequence is : [6]

$$1 \rightarrow 3 \rightarrow 5 \rightarrow 6 \rightarrow 7 \rightarrow 1.$$

(*b*) Design a circuit to convert 4-bit binary to its equivalent gray code. [6]

5. (*a*) What is ASM chart ? Give its application and explain the MUX controller method with suitable example. [7]

(*b*) Write VHDL code for 4-bit adder using structural modelling style. [6]

Or

6. (*a*) Draw the ASM chart for the following state machine. A 2-bit up counter is to be designed with output $Q_A Q_B$ and enable signal 'X'. If X = 0, then counter changes the state as 00-01-10-11-00. If 'X' = 1, then counter should remain in current state. Design the circuit using J-K flip-flop and suitable MUX. [7]

(*b*) Write a VHDL code for 8 : 1 MUX using Behavioural modeling. [6]

7. (*a*) Draw and explain basic architecture of FPGA in detail. [6]

(*b*) A combinational circuit is defined by the functions : [7]

$$f_1(A, B, C) = \Sigma m(3, 5, 7)$$

$$f_2(A, B, C) = \Sigma m(4, 5, 7)$$

Implement the circuit with PLA having 3 input and 3 product term with 2 output.

Or

8. (*a*) Implement 4 : 1 MUX using PAL. [6]

(*b*) Implement the following functions using PLA : [7]

$$f_1(A, B, C) = \Sigma m(0, 3, 4, 7)$$

$$f_2(A, B, C) = \Sigma m(1, 2, 5, 7).$$