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[5252]-168

S.E. (Computer Engineering) (Second Semester)

EXAMINATION, 2017

MICROPROCESSORS AND INTERFACING TECHNIQUES

(2012 PATTERN)

Time : 2 Hours

Maximum Marks : 50

N.B. :— (i) Answer total question Nos. 1 or 2, 3 or 4, 5 or 6,
7 or 8.

(ii) Neat diagrams must be drawn whenever necessary.

(iii) Figures to the right indicate full marks.

1. (a) What do you mean by Bus Sizing ? Draw the Memory Read.
Write cycle timing diagrams for 16 or 32 bit microprocessor.

[8]

(b) What do you mean by Directive ? Give directive which is related
to allocation of storage for one or more values ?
(minimum 6 directives)

[4]

Or

2. (a) What is DOS ? Explain any *two* internal and *two* external
DOS commands.

[4]

(b) Compare .COM and .EXE File.

[4]

(c) Explain the concept of TSR with figure.

[4]

P.T.O.

3. (a) Give difference between synchronous and asynchronous communication. [4]
(b) Draw block diagram for 8251A (VSART) and explain. [5]
(c) Define sensors and transducer. Give *one* example of each. [3]

Or

4. (a) Explain any *two* operating modes of 8253/8254. [6]
(b) Why DMA controlled data transfer are preferred over interrupt driven or program controlled and explain the use of HRQ and EOP signals ? [3]
(c) What is the difference between *n* key rollover and 2 key lock out in 8279 ? [3]
5. (a) Explain and discuss interface between 8086 and 8087. [6]
(b) Draw and explain timing diagram for read operation of 8086 in minimum mode. [7]

Or

6. (a) Explain the instruction related to 8087 : [6]
(i) FSTP
(ii) FICON
(iii) FLDZ
(iv) FIST.
(b) Define the following terms : [3]
(i) Accuracy
(ii) Monotonocity
(iii) Offset error.
(c) Explain use of 8282 and 8284. [4]

7. (a) List and explain the features of Intel X58 chipset. [7]
(b) What is the purpose of 82801JR I/O controller Hub ? List of features of same. [4]
(c) Draw basic blocks of Intel X58 chipset. [2]

Or

8. (a) Explain the basic components of *i5* processor with block diagram. [7]
(b) Explain the following components of 82801 JR I/O controller Hub : [6]
(i) Direct Media Interface
(ii) Serial peripheral Interface
(iii) Quiet System Technology.