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[5252]-573

S.E (Information Technology) (I Sem.) EXAMINATION, 2017
DIGITAL ELECTRONICS AND LOGIC DESIGN
(2012 COURSE)

Time : Two Hours

Maximum Marks : 50

N.B. :— (i) Answer Question 1 or 2, 3 or 4, 5 or 6 and 7 or 8

(ii) Neat diagrams must be drawn wherever necessary.

(iii) Figures to the right indicate full marks.

(iv) Assume suitable data if necessary.

1. (a) Explain the standard TTL characteristics in detail. [6]

(b) Convert the following binary numbers to octal then to decimal.

Show the steps of conversions. [6]

(i) 11011100.101010

(ii) 01010011.010101

(iii) 10110011

Or

2. (a) Draw and explain 4 bit Excess-3 adder using IC 7483. Also explain with example addition of numbers with carry. [6]

(b) Minimize the following function using K-map and implement using basic logic gates. [6]

$$f(A, B, C, D) = \sum m(1, 3, 5, 8, 9, 11, 15) + d(2, 13)$$

3. (a) Explain the working of magnitude comparator using IC 7485. Choose suitable inputs. [6]

(b) Design 12: 1 Mux using 4:1 multiplexer (with enable inputs). Explain the truth table of your circuit in short. [6]

P.T.O.

Or

4. (a) Explain with a neat diagram working of parallel in serial out 4-bit shift register. Draw necessary timing diagram. [6]
(b) What is Mod counter ? Explain MOD-26 counter using IC 7490. Draw design for the same. [6]
5. (a) What is ASM chart ? Draw ASM chart for 3-bit up-down counter. [6]
(b) Explain the basic architecture of FPGA. [7]

Or

6. (a) Define PLD. Implement the following function using PAL
 $F(A,B,C,D) = \sum m(0,1,3,15)$ [6]
(b) Differentiate between CPLD and FPGA. [7]
7. (a) Explain Process statement in behavior method of VHDL with respect to syntax, declarative part and statement part. [6]
(b) What is difference between concurrent and sequential statements in VHDL. [7]

Or

8. (a) What is difference between signal and variable in VHDL ? Explain with example. [6]
(b) Write a VHDL structural code for 4:1 multiplexer shown in figure. [7]

