Total No. of Questions : 12]

SEAT No. : [ ]

P2969

[Total No. of Pages : 3

[5354]-183
B.E.
COMPUTER
Advanced Computer Architecture & Computing
(2008 Pattern)

Time : 3 Hours] ***[Max. Marks :100***

Instructions to the candidates:

1) ***Answers to the two sections should be written in separate answer books.***
2) ***Answer Q1 or Q2, Q3 or Q4, Q5 or Q6 from section - I and Q7 or Q8, Q9 or Q10, Q11 or Q12 from section - II.***
3) ***Neat diagrams must be drawn wherever necessary.***
4) ***Figures to the right side indicate full marks.***
5) ***Assume Suitable data if necessary***

SECTION - I

Q1) a) Explain in brief Flynn's and Feng's Classification for parallel computer architecture. **[8]**

b) Discuss different Hazards in pipeline processor and their resolution. **[10]**

OR

Q2) a) Discuss the following different pipeline and advanced pipeline technique **[8]**

i) Register tagging.
ii) Internal forwarding.

b) State and explain the principle of scalability and different performance Metrics associated with it . Explain in brief Amdahl's law for speed up performance. **[10]**

Q3) a) What are the various features of uniprocessor system which exploits the parallelism. **[8]**

b) What is job sequencing problem with pipeling architecture? Define following terms: **[8]**

i) Forbidden list
ii) Collision vector
iii) Simple cycle
iv) Greedy cycle
v) MAL
vi) Throughput

P.T.O.

OR

Q4) a) Explain design issues of instruction and arithmetic pipeline. **[8]**

b) Discuss the vector instruction set and differenciate between vectoe and Superscalar architecture. **[8]**

Q5) a) How a 3-cube network can viewed as .Discuss in detail the parallel algorithm for matrix multiplication. Obtain the time complexity for the same. **[8]**

b) Discuss vector optimizing techniques implemented in vectorizing compiler. **[8]**

OR

Q6) a) Considering Mesh network as an interconnection network for array processors. Discuss in detail the parallel algorithm for sorting the array of elements. **[8]**

b) With suitable example explain following features implemented in cray-1 architecture. **[8]**

i) Vector chaining

ii) Strip Mining

SECTION - II

Q7) a) Discuss Dynamic bus arbitration techniques associated with time shared bus. **[10]**

b) Compare between : **[8]**

i) Write - Through and Write - Back caches

ii) Write - Update and write - Invalidate protocol.

OR

Q8) a) What is the difference between static and dynamic bus arbitration techniques. Explain any two dynamic bus arbitrations techniques. **[8]**

b) With the help of few machine instructions explain the hardware support provided for inter process synchronization. **[6]**

c) Discuss about loosely coupled multiprocessor system. **[4]**

Q9) a) State cache multi coherency problem in multiprocessor system. Describe the various state of MESI protocol. **[8]**

b) Compare cross bar switch with multiported memory module interconnection network. **[8]**

OR

Q10)a) Discuss the various context switching policies implemented in multithreaded architecture. **[8]**

b) Explain with suitable example message passing parallel programming. **[8]**

Q11)a) Define the term-memory consistency model. What different types of memory consistency models are available for multithreaded architectures? Discuss various parameters affecting performance of multithreaded architecture. **[8]**

b) Explain with suitable examples shared memory parallel programming. **[8]**

OR

Q12)a) Explain the various steps to be followed to develop parallel algorithms for multiprocessors. **[8]**

b) Compare PVM and MPI message passing libraries. Explain briefly various communication functions implemented as a part of MPI. **[8]**

❖ ❖ ❖ ❖