| Total No.     | f Questions : 10] SEAT No. :  |
|---------------|---|
| P3322         | [Total No. of Pages : 4   |
|               | [5353]-197  |
|               | T.E. (IT) (Semester - II)   |
|               | SYSTEMS PROGRAMMING   |
|               | (2012 Pattern)  |
| Time : 21/2   |   |
| Instructio    | ns to the candidates:   |
| 1)            | Answer Q1 or Q2, Q3 or Q4, Q5 or Q6, Q7or Q8, Q9 or Q10.  |
| 2)            | Neat diagrams must be drawn wherever necessary.   |
| 3)            | Figures to the right side indicate full marks.  |
| 4)            | Assume Suitable data if necessary.  |
|               |   |
| <b>Q1)</b> a) | Give the various data structures in the design of 2-pass macroprocessor. [6]  |
| b)            | Define the following: [4]   |
|               | i) Assembler  |
|               | ii) Macroprocessor  |
|               | iii) Compiler   |
|               | iv) Loader/Linker   |
|               | OR  |
|               | 9,  |
| <b>Q2)</b> a) | With the structure explain the different tables that would be generated a output of lexical analysis. [4]                         |
| b)            | What are the assembler directives? Explain how assembler directives LTORG, ORIGIN, START, END and EQU are processed with examples |
|               |   |
| <b>Q3)</b> a) | For the following piece of assembly language code, show the contents  |
|               | of symbol table, literal table and pool-tab. Assume size of instruction   |
|               | equal to one. [6]   |

START 500 MULT BREG, A

|               | MOVEM AREG, = '10'   |     |
|---------------|--|-----|
|               | LOOP MOVER AREG, A   |     |
|               | MOVER CREG,B   |     |
|               | ADD CREG, = '1'  |     |
|               | SUB CREG,A   |     |
|               | LTORG  |     |
|               | ADD CREGB'   |     |
|               | NEXT SUB AREG,='1'   |     |
|               | STOP   |     |
|               | ORIGIN 300   |     |
|               | MULT CREG, B   |     |
|               | ADS 1  |     |
|               | BACK EQU LOOP  |     |
|               | B DS 1   |     |
|               | END  |     |
| b)            | Define loader and enlist the basic functions of loader.                          | [4] |
|               | ORO  |     |
| <b>Q4)</b> a) | Explain the phases of compiler w.r.t the following statement:                    | [8] |
|               | R = (b*b-4*a*c)/(2*a)  |     |
| b)            | Define the term forward reference in an assembler.                               | [2] |
|               | Consider the grammar $E \rightarrow E-E$ $E \rightarrow E^*E$ $E \rightarrow id$ | ,   |
| <b>Q5)</b> a) | Consider the grammar   | [8] |
|               | $E \rightarrow E-E$  |     |
|               | $E \rightarrow E^*E$   |     |
|               | $E \rightarrow id$   |     |
|               | Perform shift Reduce parsing of i/p string "id – id * id"                        |     |
| b)            | Explain LEX file structure.  | [6] |
| c)            | Compare bottom up and top down parser.   | [4] |
|               | OR OR  |     |

Consider the following grammar **Q6)** a)

 $S \rightarrow iEtSS'/a$ 

 $S' \rightarrow eS/e$ 

 $E \rightarrow b$ 

Design a table driven predictive parser and parse the string 'ibtae'. [8]

- Explain YACC file structure. b) [5]
- With a neat diagram explain the classification of parsers. c) [5]

Define synthesized and inherited attributes. For the grammar given, **Q7**) a) [8]

 $F \rightarrow digit$ 

Draw the annotated parse tree for the expression 3\*5\*2 and list down the synthesized and inherited attributes.

Write the following expression in the form of postfix notation, Directed b) acyclic graph, quadruple and triple. [8]

 $a = b^* (-c) + b^* (-c)$ 

- Draw the dependency graph for the example of 7 a. *Q8*) a)
  - re. Translate the following C fragment into the three address code. b)

int i,j,k; for (i = 1; i < =5; i++)

> J=j+kT[i][j]=k\*k-1;

T[i][j]=k\*k;

}

What is the need for intermediate code generation? c)

Explain the different IC forms with examples.

[6]

[4]

**Q9)** a) Optimize the following code [8] i=1j=1t1=i \* 80 t2=j\*4 t8 = a[t7]b) Write short note on activation record. [4] Explain in brief run time storage allocation. [4] c) Generate three address code for *Q10)*a) [8] while (a<c) and (b>d) do If a = 1 then c = c +Else while (a<=d) do

- b) Explain different storage allocation strategies.
- c) Explain various code generation issues.

}