(II)

Total No. of Questions – [08]

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G.R. No.	

U218–135(ESE)

DECEMBER 2018/ENDSEM

S. Y. B. TECH. (E&TC) (SEMESTER - I)

COURSE NAME: DIGITAL ELECTRONINCS

COURSE CODE: ETUA21175

(PATTERN 2017)

Time: [**2 Hours**]

[Max. Marks: **50**]

(*) Instructions to candidates:

1) **Answer Q.1, Q.2, Q.3, Q.4, Q.5 OR Q.6, Q.7 OR Q.8**
2) **Figures to the right indicate full marks.**
3) **Use of scientific calculator is allowed**
4) **Use suitable data where ever required**

Q.1) a) Use a K-map to simplify each expression to minimum POS form: **[6]**

i) $Y = (A + \overline{B} + C + \overline{D})(\overline{A} + B + \overline{C} + D)(\overline{A} + \overline{B} + \overline{C} + \overline{D})$

ii) $Y = (X + \overline{Y})(W + \overline{Z})(\overline{X} + \overline{Y} + \overline{Z})(W + X + Y + Z)$

OR

b) Using a K-map, convert the following standard POS expression into a minimum POS expression, a standard SOP expression, and a minimum SOP expression. **[6]**

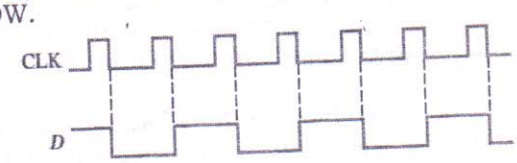
$Y = (\overline{A} + \overline{B} + C + D)(A + \overline{B} + C + D)(A + B + C + \overline{D})(A + B + \overline{C} + \overline{D})(A + B + \overline{C} + D)$

Q.2) a) Design a logic circuit to produce a HIGH output only if the input, represented by a 4-bit binary number, is greater than twelve or less than three. Write the truth table and then draw the logic diagram. **[6]**

OR

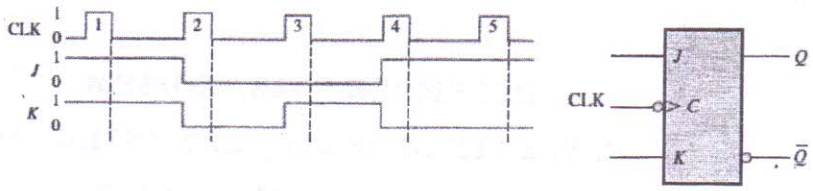
b) Develop a combinational system which has three input and produces output Y. Whenever even number of ones are detected by the system Output Y=1. Write the truth table and draw its logic diagram. **[6]**

Q.3) a) Draw the Q output relative to the clock for a D flip-flop with the inputs as shown in fig. Assume positive edge triggering and Q initially LOW. **[6]**



OR

b) The waveform in shown in fig. below is applied to the J, K, and clock inputs as indicated. Determine the Q output, assuming that the flip-flop is initially RESET. **[6]**



Q.4) a) Design a shift resistor with suitable flip-flops that will follow the sequence 1000, 0100, 0010, 0001, 0000...write its truth table and draw its logic diagram. **[4]**

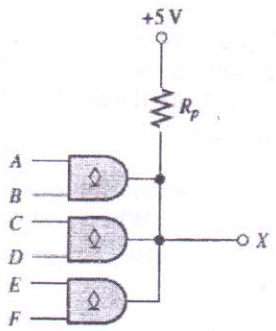
OR

b) Design a synchronous circuit using suitable flip-flop which will follow the sequence 00, 01, 10, 11, 00... write its truth table and draw its logic diagram. **[4]**

Q.5) a) A certain IC has two input CMOS NOR gates. Draw the internal diagram of CMOS NOR gate and explain its working for all the possible combination of inputs. **[6]**

b) Draw the architecture of CPLD and write its parameters. **[4]**

c) Three open-collector AND gate are connected in a wired AND configuration as shown in figure. Assume that the wired-AND circuit is driving four standard TTL inputs (-1.6 mA each). **[4]**
i) Write the logic expression for X.
ii) Determine the minimum value of R_p if $I_{OL(max)}$ for each gate is 30 mA and $V_{OL(max)}$ is 0.4 V

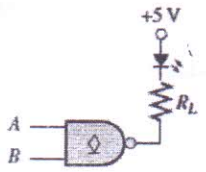


OR

Q.6) a) A certain IC has four two input TTL NAND gates. Draw the internal structure of TTL NAND gate and explain its working for all the possible combinations of inputs. **[6]**

b) A certain IC is of CMOS NOT gates. Draw the internal structure of CMOS inverter gate and explain its working for all possible combinations on input. **[4]**

c) Determine the value of the limiting resistor, R_L, in the open-collector circuit of figure if the LED current is to be 20 mA. Assume a 1.5 V drop across the LED when it is forward-biased and a LOW-state output voltage of 0.1 V at the output of the gate. [4]



Q.7) a) A long sequences of pulses enters a synchronous sequential circuit which is required to produce an output z=1, whenever the sequence 1111 occurs. Using suitable flip-flop design the non-overlapping system and draw its logic diagram. [6]

b) With suitable example explain the following terms: [4]
1. State Table 2. State diagram

c) Write truth table, excitation table for SR flip-flop and draw its state diagram [4]

OR

Q.8) a) A long sequences of pulses enters a synchronous sequential circuit which is required to produce an output z=1, whenever the sequence 1010 occurs. [6]

b) Write truth table, excitation table for JK flip-flop and draw its state diagram [4]

c) Design a sequence detector which will produce output z=1, whenever the sequence 110 occurs. Using suitable flip-flop design the non-overlapping system and draw its logic diagram. [4]