Total No. of Questions – [08] Total No. of Printed Pages- [02]

G.R. No.	

U218–125(ESE)

DECEMBER 2018/ENDSEM

S. Y. B. TECH. (COMPUTER ENGINEERING) (SEMESTER - I)

COURSE NAME: DIGITAL SYSTEMS AND LOGIC DESIGN

COURSE CODE: CSUA21175

(PATTERN 2017)

Time: [**2 Hours**] [Max. Marks: **50**]

(Marking Scheme)

Q.1) a) 4 marks for each step of truth table and 2 marks for circuit design. [6 marks]

OR

b) 1) 2 marks for De-Morgan's Theorem. [6 marks]

2) 4 marks for Boolean expression.

Q.2) a) 1) 2 marks for truth table. [6 marks]

2) 2 marks for K-maps.

3) 2 marks for logical circuit design.

OR

b) 1) 2 marks for truth table. [6 marks]

2) 2 marks for K-maps.

3) 2 marks for logical circuit design.

Q.3) a) 2 marks for explanation and 4 marks for design of MOD-96 counter. [6 marks]

OR

b) 2 marks for each differentiation. [6 marks]

Q.4) a) 2 marks for PAL & 2 marks PLA architecture. [4 marks]

OR

b) 1 mark for each application of PLD's. [4 marks]

Q. 5) a) 2 marks for VHDL definition & 4 marks for VHDL code. [6 marks]

b) 1) 2 marks for state diagram. [4 marks]
2) 4 marks for ASM chart.

c) 1 mark for ASM chart & 3 marks for explanation of Mux Controller method. [4 marks]

OR

Q.6) a) 2 marks for each difference between concurrent and sequential statements of VHDL. [6 marks]

b) 1 mark for each advantage of VHDL. [4 marks]

c) 2 mark for each comparison of ASM & VHDL. [4 marks]

Q.7) a) 2 marks for explanation & 4 marks for Arduino architecture. [6 marks]

b) 1 mark each for each step of soldiering techniques. [4 marks]

c) 1 mark for each classification of logic families. [4 marks]

OR

Q.8) a) 2 marks for each parameter to characterize logic families. [6 marks]

b) 1 mark for each application of Raspberry pi. [4 marks]

c) 2 marks each for explanation of CMOS and RTL. [4 marks]