Total No. of Questions – [04]

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PH8-142 (T1)

| G.R. No. | |
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**OCTOBER 2018 / IN - SEM (T1)**

**F. Y. M. TECH. (E&TC-Signal Processing) (SEMESTER -I)**

**COURSE NAME:** Advanced Embedded Processors and Programming

**COURSE CODE:** ETPA11182

**(PATTERN 2018)**

**Scheme of Marking**

**Q.1)**

**A) Justify the RISC architecture philosophy in advanced Processors.** **[6]**

Marking Scheme: Advanced Processors are used for control, communication and compute application in isolation or unified. Towards this RISC architecture philosophy as

1. Single cycle execution
2. Large Register bank
3. Load and store architecture
4. Effective Interrupt structure
5. Advanced pipeline for better throughput
6. Hardwired Units etc

Explanation of at least 06 features = 01 mark each

**B) Elaborate flow of software development with any one IDE.** **[4]**

Marking Scheme: software development flow diagram = 02 marks

Explanation of cross compiler, linker, loader, debugger =02 marks

**OR**

**Q.2)**

**A) What are embedded system design challenges? Justify with any one case study.** **[6]**

Marking Scheme: Any three design challenges: 03 marks

Justification /Explanation with case study: 03 marks

**B) How embedded C programming is different than C programming?** **[4]**

Marking Scheme: any four differentiation points = 04 marks (01x04)

**Q.3) Will increase in pipeline stages always results in better performance? Justify the answer.** **[10]**

Marking Scheme: any 05 pros and cons with increased pineline stages w.r.t increased throughput / pipeline hazards/ etc… (02x05 marks)

**OR**

**Q.4)**

**A) What are pipeline hazards? Which remedial measures are used to reduce hazards?** **[06]**

Marking Scheme: Three types of pipeline hazards -- 03 marks
Remedial measures --03 marks

**B) Compare sequential, concurrent and parallel programming model.** **[4]**

Marking Scheme: any four comparison points with merits and demerits – (01x04 marks)