Total No. of Questions – [04] Total No. of Printed Pages: 01

P118-142(T1)

G.R. No.	

OCTOBER 2018 / IN - SEM (T1)

F. Y. M. TECH. (E&TC-Signal Processing) (SEMESTER -I)

COURSE NAME: Advanced Embedded Processors and Programming

COURSE CODE: ETPA11182

(PATTERN 2018)

Time: [1 Hour] [Max. Marks: 20]

(*) Instructions to candidates:

1) **Answer Q.1 OR Q.2, Q.3 OR Q.4**
2) **Figures to the right indicate full marks**
3) **Use of scientific calculator is allowed**
4) **Use suitable data where ever required**

Q.1)

A) Justify the RISC architecture philosophy in advanced Processors. [6]

B) Elaborate flow of software development with any one IDE. [4]

OR

Q.2)

A) What are embedded system design challenges? Justify with any one case study. [6]

B) How embedded C programming is different than C programming? [4]

Q.3)

Will increase in pipeline stages always results in better performance? Justify the answer. [10]

OR

Q.4)

A) What are pipeline hazards? Which remedial measures are used to reduce hazards? [6]

B) Compare sequential, concurrent and parallel programming model. [4]