OCTOBER 2018/ IN-SEM (T1) U218-123(T1)

S. Y. B. TECH. (COMPUTER ENGINEERING) (SEMESTER - I)

COURSE NAME: COMPUTER ORGANIZATION AND MICROPROCESSORS TECHNIQUES

COURSE CODE: CSUA21173

(PATTERN 2017)

Marking Scheme

Q.1) a) A = 1110 Q= 0010 4 steps 1.5 Marks for each step

b) list components of computer [1 Mark]
Description [3 Marks]
Diagram [2 Marks]

c) Diagram [1 Mark]
Description [3 Marks]

Q. 2) a) A= 0010 Q= 1001 [6 Marks]

b) Definition [2Marks]
Functions of each bus [2Marks]

c) binary representation (-12), 15 [1Mark]
2's Complement method [2 Marks]
Final answer 00011 [1 Mark]

Q.3) a) Block diagram [3 Marks]
Explanation [3 Marks]

b) Any 4 differentiate points (1 Marks for each point) [4 Marks]
c) 3 Types of classification with examples [4 Marks]

Q.4) a) 5 functions with explanation [6 Marks]

b) Memory hierarchy diagram [2 Marks]
Explanation [2 Marks]

c) Meaning of Interrupt driven I/O [1 Marks]
Diagram of Interrupt driven I/O [1 Marks]
Explanation [2 Marks]

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Model Answer Paper

Q1) a) Given x=0101 and y=1010 in two's complement notation (i.e. x=5, y= - 6), compute the product [p=x*y] with Booth's Algorithm. [6 marks]

Solution :

A	Q	Q_{-1}	M	Operation	Cycle NO.
0000	1010	0	0101	Initial Value	
0000	0101	0	0101	Arithmetic shift right	1
1011	0101	0	0101	A=A-M	2
1101	1010	1	0101	Arithmetic shift right	
0010	1010	1	0101	A=A+M	3
0001	0101	0	0101	Arithmetic shift right	
1100	0101	0	0101	A=A-M	4
1110	0010	1	0101	Arithmetic shift right	

Result is in A:Q

Q1) b) List and briefly define the main structural components of a computer.

Solution : **[6 marks]**

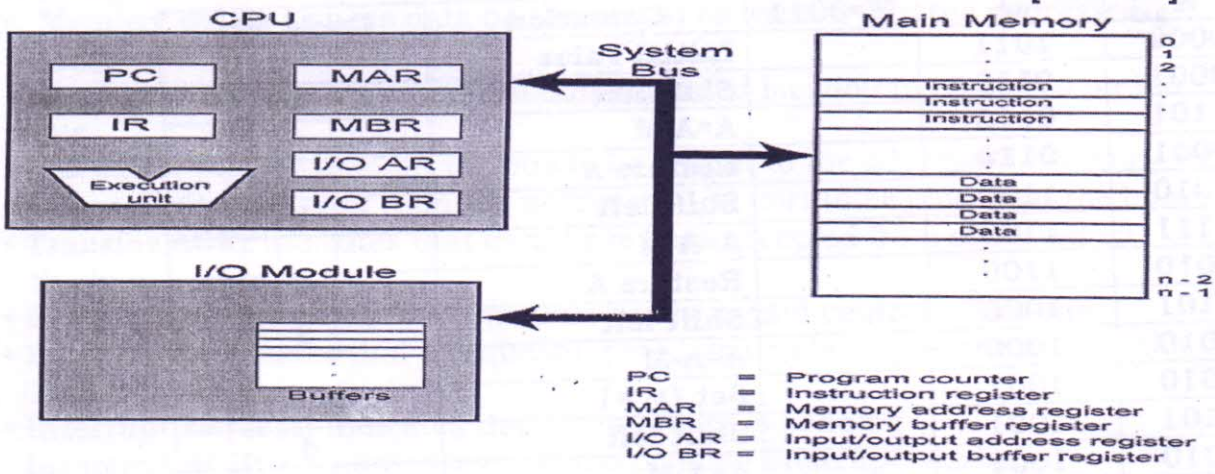

Figure : Main structural components of a computer

Brief description of following

- The Control Unit and the Arithmetic and Logic Unit constitute the Central Processing Unit

- Data and instructions need to get into the system and results out
  - — Input/output
- Temporary storage of code and results is needed
  - — Main memory

Q1) c) Describe IEEE754 standard for floating point numbers? [4 marks]
Solution:

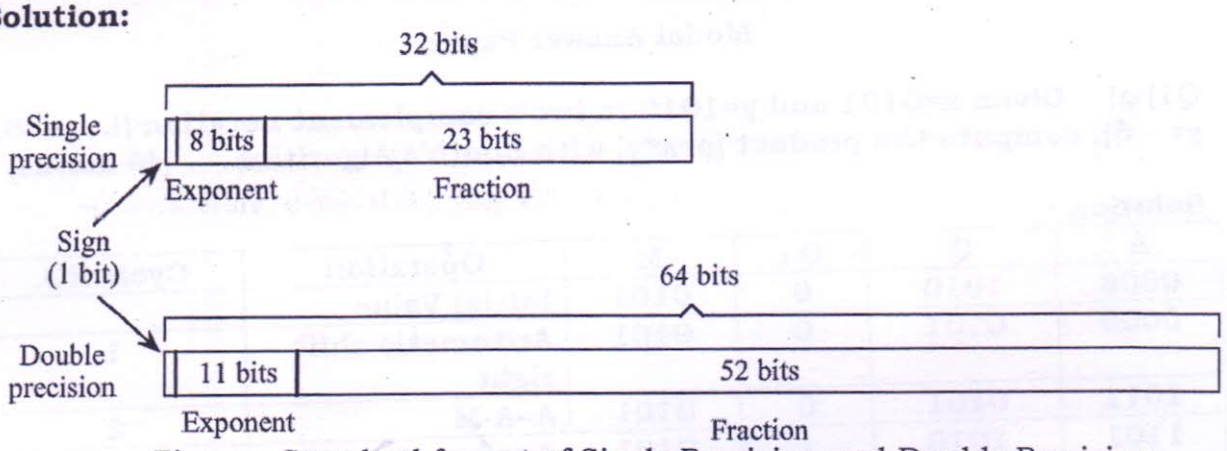

Figure : Standard format of Single Precision and Double Precision

- +/- 1.significand x 2exponent
- Standard for floating point storage
- 32 and 64 bit standards
- 8 and 11 bit exponent respectively
- Extended formats (both mantissa and exponent) for intermediate results

Q.2) a) Solve Division of the following numbers using restoring Division Algorithm: Dividend=1011, Divisor=0011. [6 marks]

Solution :

Restoring Division

A	Q	M=0011	Operation	Cycle NO.
0000	1011		Initial Value	
0001	0110		Shift left	1
1101	0110		A=A-M	
0001	0110		Restore A	
0010	1100		Shift left	2
1111	1100		A=A-M	
0010	1100		Restore A	
0101	1000		Shift left	3
0010	1000		A=A-M	
0010	1001		Set Q_0 =1	
0101	1001		Shift left	4
0010	1001		A=A-M	
0010	1001		Set Q_0 =1	

Quotient is in Q and Remainder in A

Q.2) b) What is a bus? What are the functions of data, address and control bus? [6 marks]

Solution :

BUS:- A communication pathway connecting two or more devices

- Usually broadcast
- Often grouped
  - — A number of channels in one bus
  - — e.g. 32 bit data bus is 32 separate single bit channels
- Power lines may not be shown

1) Data Bus:- Carries data
   The **data lines** provide a path for moving data among system modules. These lines, collectively, are called the *data bus*.The data bus may consist of 32, 64, 128, or even more separate lines, the number of lines being referred to as the *width* of the data bus.
2) Address Bus:- Identify the source or destination of data
   The **address lines** are used to designate the source or destination of the data on the data bus.
   For example, if the processor wishes to read a word (8, 16, or 32 bits) of data from memory, it puts the address of the desired word on the address lines.
   Clearly, the width of the address bus determines the maximum possible memory capacity of the system. Furthermore, the address lines are generally also used to address I/O ports.
3) Control Bus:- Identify the source or destination of data

The **control lines** are used to control the access to and the use of the data and address lines.

Control signals transmit both command and timing information among system modules.

Timing signals indicate the validity of data and address information. Command signals specify operations to be performed.

Typical control lines include

- **Memory write:** Causes data on the bus to be written into the addressed location
- **Memory read:** Causes data from the addressed location to be placed on the bus
- **I/O write:** Causes data on the bus to be output to the addressed I/O port
- **I/O read:** Causes data from the addressed I/O port to be placed on the bus
- **Transfer ACK:** Indicates that data have been accepted from or placed on the bus
- **Bus request:** Indicates that a module needs to gain control of the bus
- **Bus grant:** Indicates that a requesting module has been granted control of the bus
- **Interrupt request:** Indicates that an interrupt is pending
- **Interrupt ACK:** Acknowledges that the pending interrupt has been recognized
- **Clock:** Is used to synchronize operations
- **Reset:** Initializes all modules

Q.2) c) Compute the following using 2's Complement method (-12 +15). **[4 marks]**

Solution :

+12 = 01100 **2's Complement** (-12)= 10011 +1 =10100
+15 = 01111

```
    01111
+   10100
-----------
   100011
```

Carry generated is ignored so answer is 00011 i.e. 3

Q.3) a) Draw and explain the block diagram of an External device. [6 marks]

Solution:

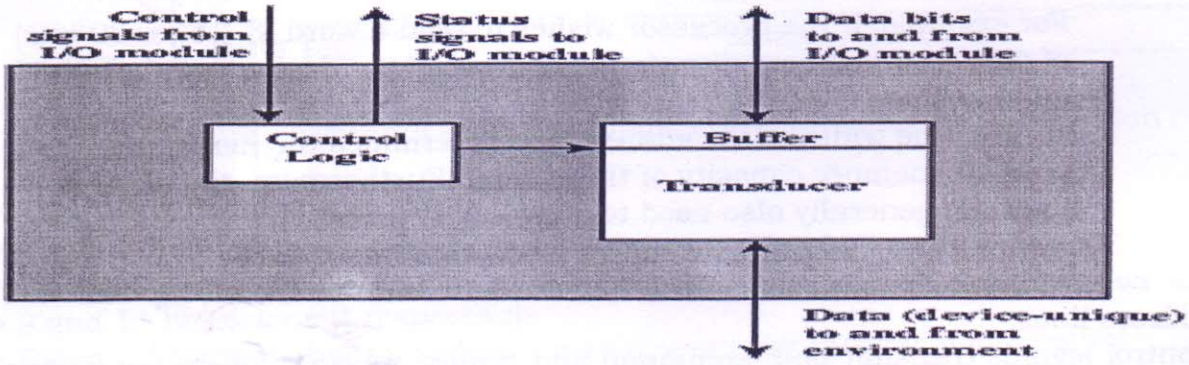

Figure: Block Diagram of External Device

- The interface to the I/O module is in the form of control, data and status signal.
- Control signals determine the function that the device will perform, such as send data to the I/O module (INPUT or READ), accept data from the I/O module (OUTPUT or WRITE), report status or perform some control function particular to the device (eg. position a disk head).
- Data are in the form of a set of bits to be sent to or received from the I/O module.
- Status signals indicate the state of the device.
- Examples are READY/NOT-READY to show whether the device is ready for data transfer.
- Control logic associated with the device controls the device's operation in response to direction from the I/O module.
- The transducer converts data from electrical to other forms of energy during output and from other forms to electrical during input.

- A buffer is associated with the transducer to temporarily hold data being transferred between the I/O module and the external environment; a buffer size of 8 to 16 bits is common.

Q.3) b) Distinguish between programmed I/O and interrupt driven I/O. **[4 marks]**

Solution:

Sr. No.	Programmed I/O	Interrupt Driven I/O
1	In programmed I/O, processor has to check each I/O device in sequence and in effect 'ask' each one if it needs communication with the processor. This checking is achieved by continuous polling cycle and hence processor cannot execute other instructions in sequence.	External asynchronous input is used to tell the processor that I/O device needs is service and hence processor does not have check whether I/O device needs it service or not.
2	During Polling processor is busy and therefore have serious and decremental effect on system throughput.	In interrupt driven I/O, the processor is allowed to execute its instruction in sequence and only stop to service I/O device when it is told to do so by the device itself. This increases system throughput.
3	It is implemented without interrupt hardware support.	It is implemented using Interrupt hardware support.
4	It does not depend on interrupt status.	Interrupt must be enabled to process interrupt driven I/O.
5	It does not need initialization of stack.	It needs initialization of stack.
6	System throughput decreases as number of I/O devices connected in the system increases.	System throughput does not depend on number of I/O devices connected in the system.

Q.3) c) Explain the classification of External Devices. **[4 marks]**

Solution: External devices can be broadly classified into three categories:

- **Human readable:** Suitable for communicating with the computer user. Examples of human-readable devices are video display terminals (VDTs) and printers.
- **Machine readable:** Suitable for communicating with equipment. Examples of machine-readable devices are magnetic disk and tape systems, and sensors and actuators, such as are used in a robotics application.
- **Communication:** Suitable for communicating with remote devices.

Communication devices allow a computer to exchange data with a remote device,

which may be a human-readable device, such as a terminal, a machine-readable device, or even another computer.

Q.4) a) Explain the function of I/O module. **[6 marks]**

Solution:

The major functions or requirements for an I/O module fall into the following categories:

- Control and timing
- Processor communication
- Device communication
- Data buffering
- Error detection

During any period of time, the processor may communicate with one or more external devices in unpredictable patterns, depending on the program's need for I/O.

The internal resources, such as main memory and the system bus, must be shared among a number of activities, including data I/O.

1) **Control and Timing** : the I/O function includes a **control and timing** requirement, to coordinate the flow of traffic between internal resources and external devices.

For example, the control of the transfer of data from an external device to the processor might involve the following sequence of steps:

- The processor interrogates the I/O module to check the status of the attached device.
- The I/O module returns the device status.
- If the device is operational and ready to transmit, the processor requests the transfer of data, by means of a command to the I/O module.
- The I/O module obtains a unit of data (e.g., 8 or 16 bits) from the external device.
- The data are transferred from the I/O module to the processor.

If the system employs a bus, then each of the interactions between the processor and the I/O module involves one or more bus arbitrations.

2) Processor communication involves the following:

- **Command decoding:** The I/O module accepts commands from the processor, typically sent as signals on the control bus. For example, an I/O module for a disk drive might accept the following commands: READ SECTOR, WRITE SECTOR, SEEK track number, and SCAN record ID.
- **Data:** Data are exchanged between the processor and the I/O module over the data bus.
- **Status reporting:** Because peripherals are so slow, it is important to know the status of the I/O module. For example, if an I/O module is asked to send data to the processor (read), it may not be ready to do so because it is still working on the previous I/O command. This fact can be reported with a status signal. Common status signals are BUSY and READY. There may also be signals to report various error conditions.
- **Address recognition:** Just as each word of memory has an address, so does each I/O device. Thus, an I/O module must recognize one unique address for each peripheral it controls.

3) Device Communication: The I/O module must be able to perform **device communication**. This communication involves commands, status information, and data.

4) Data Buffering: An essential task of an I/O module is **data buffering**. The transfer rate into and out of main memory or the processor is quite high, the rate is orders of magnitude lower for many peripheral devices and covers a wide range.
Data coming from main memory are sent to an I/O module in a rapid burst.
The data are buffered in the I/O module and then sent to the peripheral device at its data rate.
In the opposite direction, data are buffered so as not to tie up the memory in a slow transfer operation.
Thus, the I/O module must be able to operate at both device and memory speeds. Similarly, if the I/O device operates at a rate higher than the memory access rate, then the I/O module
performs the needed buffering operation.

5) Error Detection: an I/O module is often responsible for error detection and for subsequently reporting errors to the processor. One class of errors includes mechanical and electrical malfunctions reported by the device (e.g., paper jam, bad disk track).
Another class consists of unintentional changes to the bit pattern as it is transmitted from device to I/O module. Some form of error-detecting code is often used to detect transmission
errors.
A simple example is the use of a parity bit on each character of data.
For example, the IRA character code occupies 7 bits of a byte.
The eighth bit is set so that the total number of 1s in the byte is even (even parity) or odd (odd parity).
When a byte is received, the I/O module checks the parity to determine whether an error has occurred.

Q.4) b) What is the general relationship among access time, memory cost, and capacity? [4 marks]

Solution:
There is a trade-off among the three key characteristics of memory: namely, capacity, access time, and cost.
A variety of technologies are used to implement memory systems, and across this spectrum of technologies, the
following relationships hold:

- Faster access time, greater cost per bit
- Greater capacity, smaller cost per bit
- Greater capacity, slower access time

The designer would like to use memory technologies that provide for large-capacity memory, both because the capacity is needed and because the cost per bit is low. However, to meet performance requirements, the designer needs to use expensive, relatively lower-capacity memories with short access times.

The way out of this dilemma is not to rely on a single memory component or technology, but to employ a **memory hierarchy**.
A typical hierarchy is shown in Figure. As one goes down the hierarchy, the following occur:
a. Decreasing cost per bit
b. Increasing capacity
c. Increasing access time
d. Decreasing frequency of access of the memory by the processor
Thus, smaller, more expensive, faster memories are supplemented by larger, cheaper, slower memories. The key to the success of this organization is item (d): decreasing frequency of access.

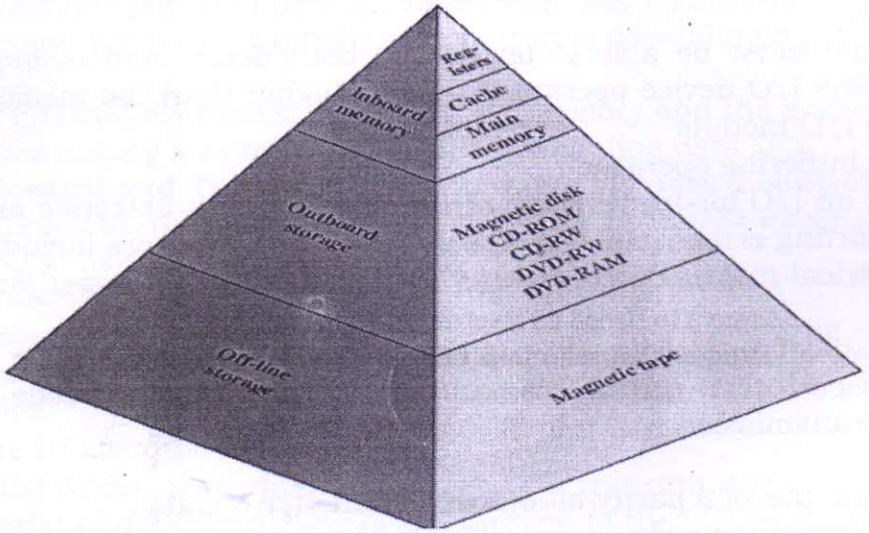

Figure: The Memory Hierarchy

Q.4) c) Explain Interrupt driven I/O. [4 marks]

Solution:

Interrupt driven I/O is an alternative scheme dealing with I/O.
Interrupt I/O is a way of controlling input/output activity whereby a peripheral or terminal that needs to make or receive a data transfer sends a signal.
This will cause a program interrupt to be set. At a time appropriate to the priority level of the I/O interrupt.
Relative to the total interrupt system, the processors enter an interrupt service routine.
The function of the routine will depend upon the system of interrupt levels and priorities that is implemented in the processor.

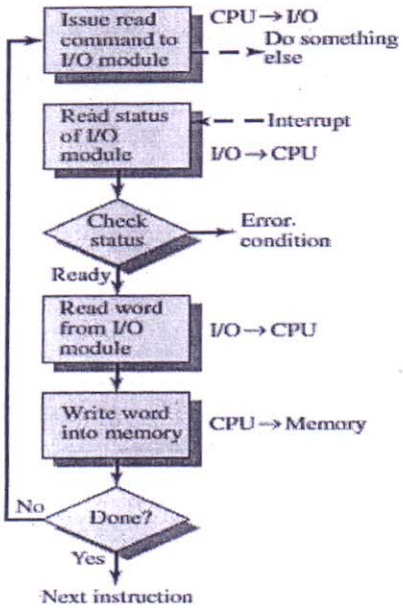

Figure: Interrupt Driven I/O

Interrupt Processing

1. A device driver initiates an I/O request on behalf of a process.
2. The device driver signals the I/O controller for the proper device, which initiates the requested I/O.
3. The device signals the I/O controller that is ready to retrieve input, the output is complete or that an error has been generated.
4. The CPU receives the interrupt signal on the interrupt-request line and transfer control over the interrupt handler routine.
5. The interrupt handler determines the cause of the interrupt, performs the necessary processing and executes a "return from" interrupt instruction.
6. The CPU returns to the execution state prior to the interrupt being signalled.
7. The CPU continues processing until the cycle begins again.