Total No. of Questions – [04]

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U218-125(T1)

G.R. No.	

OCTOBER 2018/ IN-SEM (T1)

S. Y. B. TECH. (COMPUTER ENGINEERING) (SEMESTER - I)

COURSE NAME: DIGITAL SYSTEMS AND LOGIC DESIGN

COURSE CODE: CSUA21175

(PATTERN 2017)

Time: [**1 Hour**] [Max. Marks: **30**]

Instructions to candidates:

1) **Answer Q.1 OR Q.2 and Q.3 OR Q.4.**
2) **Figures to the right indicate full marks.**
3) **Use of scientific calculator is allowed**
4) **Use suitable data wherever required**

Q 1) a) Minimize logic function using K-map and implement it using logic gates.

$Y(A, B, C, D) = \Sigma m(0, 1, 2, 3, 5, 7, 8, 9, 11, 14)$ [6]

b) Simplify the four – variable Boolean function using Quine –McCluskey Methods.

$Y(A, B, C, D) = \Sigma m(2, 4, 5, 9, 12, 13)$ [6]

c) Convert decimal number $(109.125)_{10}$ to their binary equivalents. [4]

OR

Q2) a) Reduce function using K-map technique and implement using basic gates. $Y(A, B, C, D) = A'B'D + ABC'D' + BCD$ [6]

b) Simplify function using Quine-McCluskey method

$Y(A,B,C,D) = \Pi M(1,4,6,9,10,11,14,15)$ [6]

c) Represent $(64)_{10}$ in 2's complement using 8 bits. [4]

Q3) a) Design 4-bit BCD to excess-3 code conversion with truth table, k-map and logic circuit. [6]

b) Implement 8:1 Mux using a 4:1 and 2:1 Mux. [4]

c) Implement 2 Bit Comparator along with truth table, k-map and logic diagram using gates. [4]

OR

Q4) a) Implement Boolean expression using multiplexer [6]

Y=A'BC'+AB'C'D+A'B'D+A'CD

b) Design a full-adder using 3-to-8-line decoder. [4]

c) Implement 4-bit even parity generator along with truth table, k-map and logic diagram using gates. [4]