Total No. of Questions – [4] Total No. of Printed Pages 02

G.R. No. Paper Code - U218-135 (T1)

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S. Y. B. TECH. (E&TC) (SEMESTER - I)

COURSE NAME: Digital Electronics

COURSE CODE: ETUA21175

(PATTERN 2017)

Time :[1 Hour] **[Max. Marks : 30]**

(*) Instructions to candidates:

1) **Answer Q.1 OR Q.2, Q.3 OR Q.4**
2) **Figures to the right indicate full marks.**
3) **Use of scientific calculator is allowed**
4) **Use suitable data where ever required**

Q1 **a)** Simplify the given function using Quine-McClusky minimization technique **[6]**

$$f(A, B, C, D) = \sum m(0,1,2,3,5,7,8,9,11,14)$$

b) Minimize the following function using K-map **[6]**

$$Y = \sum m(0,1,4,5,6,7,9) + d(8,11,12,13,15)$$

c) Develop the logic circuit necessary to meet the following requirements: **[4]**
A battery-powered lamp in a room is to be operated from two switches, one at the back door and one at the front door. The lamp is to be on if the front switch is on and the back switch is off, or if the front switch is off and the back switch is on. The lamp is to be off if both switches are off or if both switches are on. Let a HIGH output represent the on condition and a LOW output represent the off condition.

OR

Q2 **a)** Simplify the given function using Quine-McClusky minimization technique

$$f(A, B, C, D) = \sum m(0,1,3,7,8,9,11,15)$$ **[6]**

b) Minimize the following function using K-map **[6]**

$$Y = \Pi M(0,2,4,5,6,8,10,12,13,14) + d(7,15)$$

c) Design a logic circuit to produce a HIGH output only if the input, represented by a 4-bit binary number, is greater than twelve or less than three. First develop the truth table and then draw the logic diagram. **[4]**

Q3 a) You wish to detect only the presence of the codes 0100, 1100, 0001 and 1011. An Active high o/p is read to indicate their presence. Develop minimization decoding logic with single o/p that will indicate only anyone these code are i/p. Write the truth table and draw its logic diagram [6]

b) Design 4-bit Binary to gray code converter and draw its logic diagram using XOR gates. [4]

c) Simplify the given expression using single 16:1 MUX, [4]

$$Y=\Sigma m(1,2,4,5,7,9,10,13,15)$$

OR

Q4 a) Design 4-bit Gray to Binary code converter and draw its logic diagram using XOR gates. [6]

b) Each of the eight full-adders in an 8-bit parallel ripple carry adder exhibits the following propagation delay. [4]

A to Σ and Cout: 20 ns
B to Σ and Cout: 20 ns
Cin to Σ : 30 ns
Cin to Cout: 25

Determine total time for addition of two 8-bit numbers. Justify your answer.

c) Write truth table for full substractor, solve for difference and borrow using K- map and Draw logic diagram using logic gates. [4]