Marking Scheme

OCTOBER 2018/IN-SEM (T1)

S. Y. B. TECH. (PROGRAM) (SEMESTER - I)

COURSE NAME: Semiconductor Devices and Circuits

COURSE CODE:ETUA21174

(PATTERN 2017) U218-134 (T1)

Q.NO	Sub Q.NO	Marking Scheme	Marks	Difficulty Level	Cognitive level	CO Mapped
Q1	a)	Vth=1.33V and Rth=4.44K IB=15.73μA [2] IC=0.944 mA [2] VCE= 6.32V [2]	[6]	M	Analysis	CO1
	b)	Explanation of the need of bias stabilization [3] Derivation for stability factor S for voltage divider biasing circuit. [3]	[6]	M	Comprehension	CO1
	c)	Draw h parameter model of CE amplifier [2] state the significance of each parameter. [2]	[4]	L	Comprehension	CO1
		OR				
Q2	a)	Compare CE, CB and CC amplifier	[6]	M	Comprehension	CO1
	b)	R_{th}=2.67K V_{th}=4V I_B=61.49μA [2] Ic=3.07mA [2] V_{CE}=5.79 [2]	[6]	H	Analysis	CO1
	c)	Explanation of thermal runaway	[4]	M	Knowledge	CO1
Q3	a)	Av= -6.19 [2] Ri= 1Mohm [2] Ro=3.09K [2]	[6]	H	Analysis	CO2
	b)	g_m=3.33 mS [2] I_D=8.34mA [2]	[4]	M	Analysis	CO2
	c)	Draw neat drain characteristic and transfer characteristic	[4]	L	Comprehension	CO2
		OR				

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Q4	a)	I_D=1.51 mA V_{DS}=8.63V V_{GS}= -2.26V	[2] [2] [2]	[6]	M	Analysis	CO2
	b)	Draw the ac equivalent circuit Derive expression for voltage gain: Derive expression for Ri Derive expression for Ro	[1] [1] [1] [1]	[4]	L	Analysis	CO2
	c)	Justification for each statement 2M		[4]	M	Comprehension	CO2

October 2018 / IN SEM (T_1)

S.Y. B.Tech (E&TC) Sem. I

Course :- SDC

course code :- ETUA 21174

(Pattern - 2017)

Q1. a) Data given - $V_{CC} = 12V$, $R_1 = 40k$, $R_2 = 5k$, $R_C = 5k$, $R_E = 1k$

$\beta = 60$

Solution :- $V_{Th} = \dfrac{5k\Omega}{(5k+40k)} \times V_{CC} = \dfrac{R_2}{R_1+R_2} \times V_{CC}$

$\boxed{V_{Th} = 1.33\ V}$

$R_{Th} = R_1 \| R_2 = \dfrac{5 \times 40}{5+40} = \underline{4.44\ k\Omega}$

Apply KVL to base emitter loop.

$V_{Th} = I_B R_B + V_{BE} + I_E R_E$

But $I_E = (1+\beta) I_B = 61\ I_B$

$\therefore 1.33 = 4.44k \cdot I_B + 0.7 + 61k\ I_B$

$\therefore \boxed{I_B = 15.43\ \mu A}$ ------------- [2]

$I_C = \beta I_B = 60 \times 15.43 \times 10^{-6}$

$\boxed{I_C = 0.944\ mA}$ ------------- [2M]

$V_{CE} = V_{CC} - I_C R_C - I_E R_E$

$\boxed{V_{CE} = 6.32 V}$ ------------- [2M]

b) Need of bias - stabilization

Bias stabilization is a process of stabilizing the Q point. of the circuit. Hence we need to design biasing circuit which will keep the position of Q point stable on the load line.

Due to increase of tempreture following parameters of the transistor will change -

1) V_{BE} 2) β 3) I_{CO}

1) The Base to emitter voltage decreases at a rate of 2.5 mV/°C with increase in temp. The base current I_B is increase & it will force I_C to change.

2) $\beta \rightarrow$ The current gain β of transistor is temp. dependent. As $I_C = \beta I_B$.

3) change in I_{CO} i.e reverse saturation current with temp. increase.

$$I_C = \beta I_B + (1+\beta) I_{CBO}.$$

Derivation for stability factor 'S'

$$S = \left.\frac{\Delta I_C}{\Delta I_{CO}}\right| V_{BE} \;\&\; \beta \text{ const.}$$

For CE configuration

$$I_C = \beta I_B + I_{CEO} = \beta I_B + (1+\beta) I_{CBO}.$$

$$\Delta I_C = \beta \Delta I_B + (1+\beta) \Delta I_{CBO}$$

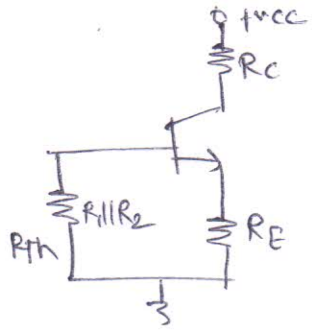
$$1 = \beta\left(\frac{\Delta I_B}{\Delta I_C}\right) + (1+\beta)\left[\frac{\Delta I_{CBO}}{\Delta I_C}\right]$$

$$1 - \beta\left[\frac{\Delta I_B}{\Delta I_C}\right] = (1+\beta)\left[\frac{\Delta I_{CBO}}{\Delta I_C}\right]$$

$$\frac{\Delta I_{CBO}}{\Delta I_C} = \frac{1-\beta(\Delta I_B/\Delta I_C)}{(1+\beta)}$$

$$\therefore \boxed{S = \frac{1+\beta}{1-\beta(\Delta I_B/\Delta I_C)}}$$

consider Thevinin's equivalent circuit.



$$V_{Th} = I_B R_B + V_{BE} + (I_C + I_B) R_E$$

Diff. w.r.t I_C

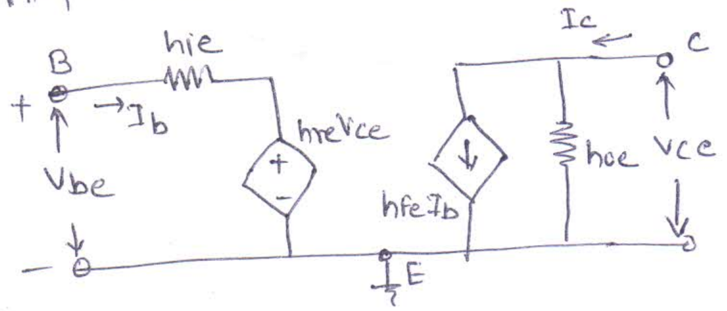
$$\therefore 0 = R_B \cdot \frac{\partial I_B}{\partial I_C} + 0 + R_E + R_E \frac{\partial I_B}{\partial I_C}$$

$$\therefore \boxed{\frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_B + R_E}}$$

$$\therefore S = \frac{1+B}{1 - B\left[\frac{-R_E}{R_B + R_E}\right]}$$

$$\therefore \boxed{S = (1+B) \frac{1 + (R_B/R_E)}{(1+B) + R_B/R_E}}$$

c) H-parameter model of CE amplifier.



1) hie = input impedance $= \left.\frac{V_{be}}{i_b}\right|_{V_{ce}=0}$

2) hfe = Forward current gain $= \left.\frac{I_c}{I_b}\right|_{V_{ce}=0}$

3) hre = Reverse voltage gain $= \left.\frac{V_{be}}{V_{ce}}\right|_{I_b=0}$

4) hoe = output admittance $= \left.\frac{I_c}{V_{ce}}\right|_{I_b=0}$

Q.2 a) compare CE, CB & CC amplifier

Parameters	CE	CB	CC
1) i/p terminal	→ Base	emitter	Base
2) o/p terminal	→ Collector	Collector	Emitter.
3) common terminal	→ Emitter	Base	collector
4) i/p resistance	→ Medium	Low	high.
5) o/p resistance	→ Medium	High	low
6) current gain	→ High	less than 1	High.
7) voltage gain	→ High	High	less than 1
8) Appln.	→ AF voltage Amplifier	Pre-amplifier	Buffer.

b)

$R_B = R_1 \| R_2 = 2.67\,k\Omega$

$V_{Th} = \frac{R_2}{R_1+R_2} \times V_{CC} = 4V$

$I_B = \frac{V_{Th} - V_{BE}}{R_B + (1+\beta) \cdot R_E}$

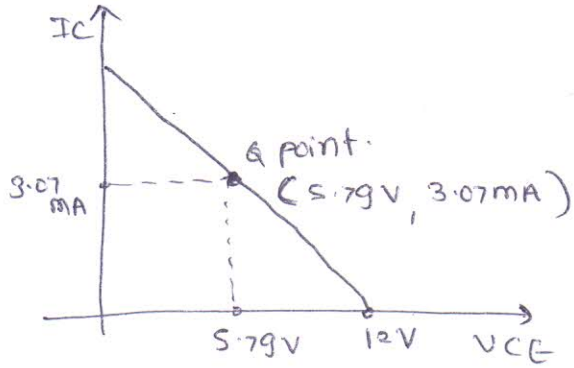
$\boxed{I_B = 61.49\,\mu A}$

$I_{CQ} = \beta I_B = 50 \times 69.49 \times 10^{-6} = 3.07\,mA$

$\boxed{I_{CQ} = 3.07\,mA}$

$V_{CEQ} = V_{CC} - I_C R_C - I_E R_E$

$\boxed{V_{CEQ} = 5.79V}$



c) Thermal run away :-

The rise in collector to base junction takes place due to two reasons-

1) increase of ambient temperature.
2) Due to internal heating.

Out of these internal heating process is cumulative as follow

1) An increase in ~~ambient temp~~. collector current I_C increases the power dissipated in the collector-base junction
2) This will increase the temp of C-B junction.
3) As transistor is NTC device causes increase temp. reduces internal resiston
4) The reduced resistance will increase the I_C further,

This is cumulative process which will finally damage the transistor due to excessive internal heating. This is known as thermal runaway.

Q3 a) For with bypass Cs amplifier using JFET

$$A_v = -g_m (R_D \| r_d)$$

$$\therefore g_{mo} = \frac{2 I_{DSS}}{V_P} = \frac{32\ mA}{8\ V} = 4\ mA/V$$

$$g_m = \cancel{\frac{I_{DSS}}{}} g_{mo} \left(1 - \frac{V_{GS}}{V_P}\right) = \cancel{4}4\left(1 - \frac{-4}{-8}\right) = 2\ mA/V$$

$$\therefore \boxed{A_v = -6.19}$$

$$\boxed{R_i = R_G = 1\ M\Omega}$$

$$\boxed{R_o = R_D \| r_d = 3.09\ k\Omega}$$

b) Given - $I_{DSS} = 12\ mA$ $V_P = -6V$, $V_{GS} = -2V$

$$\therefore g_{mo} = \frac{2 I_{DSS}}{|V_P|} = \frac{24\ mA}{6} = 4\ mA/V$$

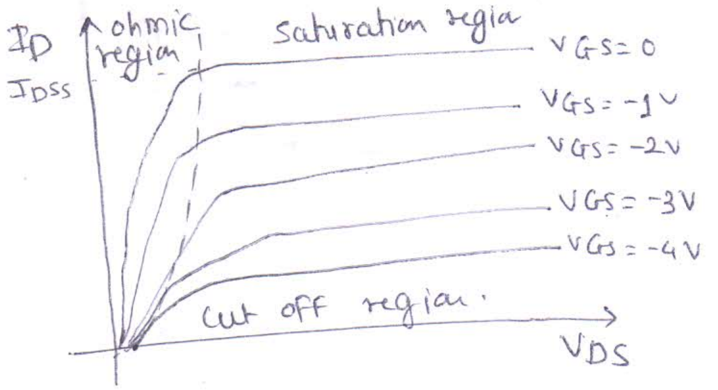
$$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right) = 4\left(1 - \frac{-2}{-6}\right)$$

$$\boxed{g_m = 3.33\ mS}$$

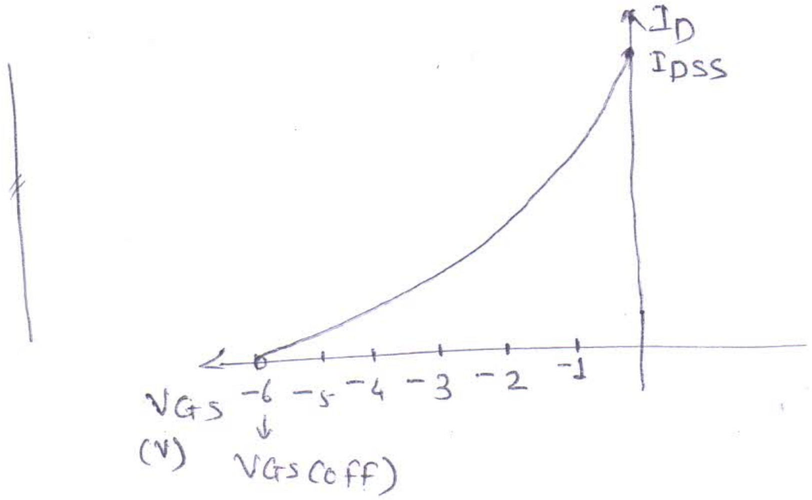
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$\boxed{I_D = 8.34\ mA}$$

c) Drain characteristics of n-channel JFET.



Transfer characteristic



Q4 a) $V_{DD} = 18\,V$, $R_D = 4.7k$ $R_S = 1.5k$ $R_G = 1M$

$V_P = -4V$ $I_{DSS} = 8\,mA$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$V_{GS} = V_G - V_S$$

$$V_{GS} = -I_D \cdot R_S$$

$$\therefore I_D = 8\times10^{-3}\left(1 - \frac{-I_D \times 1.5k}{-4}\right)^2$$

$$I_D = 8\times10^{-3}\left(1 - \frac{1500 \cdot I_D}{4}\right)^2$$

After solving quadratic equation

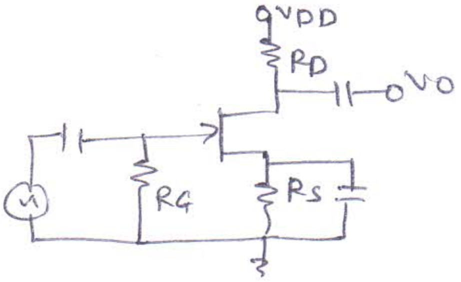
$$\boxed{I_D = 1.51\,mA}$$

$$V_{DS} = V_{DD} - I_D R_D - I_D R_S$$

$$\boxed{V_{DS} = 8.63\,V}$$

$$\boxed{V_{GS} = -I_D R_S = -2.26\,V}$$

b) Deriere expression for with bypass CS amplifier.



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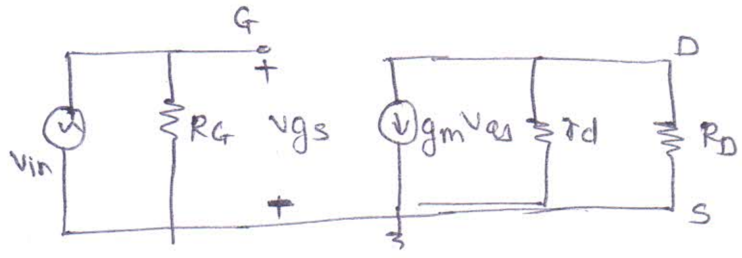

$A_V = \frac{V_o}{V_{in}}$ But $V_o = -g_m V_{gs}(r_d \| R_D)$

& $V_{in} = +V_{gs}$

$$\therefore A_V = \frac{V_o}{V_{in}} = \frac{-g_m V_{gs}(r_d \| R_D)}{V_{gs}} = \underline{-g_m(r_d \| R_D)}$$

$R_i = R_G$ = I/P impedance.

$R_o = r_d \| R_D$

c) Justify following

i) JFET is a voltage controlled device.

JFET gate current $I_g = 0$ and the voltage between gate to source is used to control current flowing thr' output terminal. V_{gs} control the drain current

$$\boxed{g_m = \frac{I_d}{V_{gs}}}$$

2) The i/p resistance of JFET is higher than BJT.

According to construction of JFET, it's input current is zero. so it having very high i/p resistance. where a BJT is a current controlled device.

As $I_C = \beta I_B$. output collecter current is function of base current. so it's i/p resistance is less.