Marking scheme

Total No. of Questions – [04]

Total No. of Printed Pages 02

U218-125(T2)

G.R. No.	

OCTOBER 2018/ IN-SEM (T2)

S. Y. B. TECH. (COMPUTER ENGINEERING) (SEMESTER - I)

COURSE NAME: DIGITAL SYSTEMS AND LOGIC DESIGN

COURSE CODE: CSUA21175

(PATTERN 2017)

Time: [**1 Hour**] [Max. Marks: **30**]

[Marking Scheme]

Q 1) a) Design a 3-bit synchronous counter using J-K flip-flops. [6]

1. Truth Table: 2 Marks
2. Kmaps & Expressions: 2 Marks
3. Logical Circuit Diagram: 2 Marks

b) Conversion of S-R flip-flop to J-K flip-flop. [6]

1. Truth Table: 2 Marks
2. Kmaps & Expressions: 2 Marks
3. Logical Circuit Diagram: 2 Marks

c) Design a 3 bit ring counter and twisted ring counter [4]

1. Ring Counter Design: 2 Marks
2. Twisted Ring Counter Design: 2 Marks

OR

Q2) a) Design MOD-96 & MOD-7 counter using 7490 ICs. [6]

1. MOD-96 Design: 4 Marks
2. MOD-7 Design: 2 Marks

b) Design a moore machine for a sequence 1110. [6]

1. State Diagram: 2 Marks
2. State Table: 1 Mark
3. Kmaps & Expressions: 2 Marks
4. Logical Circuit Diagram: 1 Mark