Total No. of Questions – [04] Total No. of Printed Pages 02

G.R. No.	

OCTOBER 2018/ IN-SEM (T2) U218-125(T2)

S. Y. B. TECH. (COMPUTER ENGINEERING) (SEMESTER - I)

COURSE NAME: DIGITAL SYSTEMS AND LOGIC DESIGN

COURSE CODE: CSUA21175

(PATTERN 2017)

Time: [**1 Hour**] [Max. Marks: **30**]

Instructions to candidates:

1) **Answer Q.1 OR Q.2 and Q.3 OR Q.4.**
2) **Figures to the right indicate full marks.**
3) **Use of scientific calculator is allowed**
4) **Use suitable data wherever required**

Q 1) a) Design a 3-bit synchronous counter using J-K flip-flops. [6]

b) Conversion of S-R flip-flop to J-K flip-flop. [6]

c) Design a 3 bit ring counter and twisted ring counter [4]

OR

Q2) a) Design a divide by 96(MOD-96) counter using 7490 ICs. [6]

b) Design a moore machine for a sequence 1110. [6]

c) Design a Master-Slave Flip-Flop using J-K flip-flop. [4]

Q3) a) Design a full adder circuit using PLA having three inputs, eight product terms, and two outputs. [6]

b) Implement a PLA for the given table [4]

PLA Program Table						
		Inputs			Outputs	
Term	Term#	A	B	C	F_1	F_2
$A\bar{B}$	1	1	0	_	1	_
AC	2	1	_	1	1	1
BC	3	_	1	1	_	1
$\bar{A}B\bar{C}$	4	0	1	0	1	_
					T	C

c) Draw structural architecture of PLA & PAL. [4]

OR

Q4) a) Implement f1(x2, x1) = Σm(0,3), f2(x2, x1) = $\overline{x2+x1}$, and f3(x2, x1) = ΠM(1) with a 4 X 3 ROM. [6]

b) What are types of PLD's? Draw structural diagram for any 3. [4]

c) Design ROM as PLD for 4 X 2 ROM. [4]