U218-135(T2)

Total No. of Questions – [4] Total No. of Printed Pages 03

G.R. No.

OCTOBER 2018/IN-SEM (T2)

S. Y. B. TECH. (PROGRAM) (SEMESTER - I)

COURSE NAME: Digital Electronics

COURSE CODE: ETUA21175

(PATTERN 2017)

Time :[1 Hour] **[Max. Marks: 30]**

(*) Instructions to candidates:

1) **Answer Q.1 OR Q.2, Q.3 OR Q.4**
2) **Figures to the right indicate full marks.**
3) **Use of scientific calculator is allowed**
4) **Use suitable data where ever required**

Q1 a) Two edge-triggered J-K flip-flops are shown in fig. b and fig. c. If the inputs are as shown in fig. a, draw the Q output of each flip-flop relative to the clock, explain the difference between the two. The flip-flops are initially Reset. **[6]**

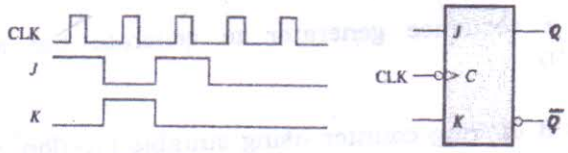
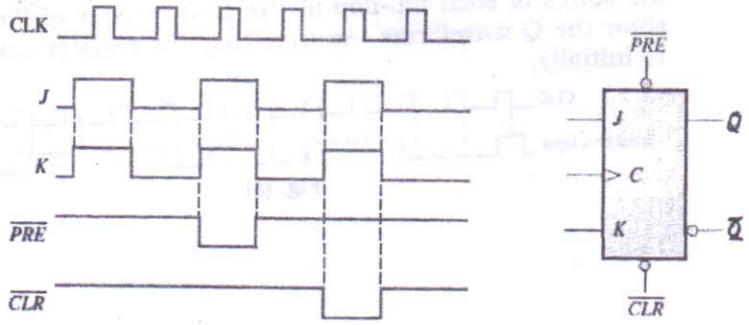


Fig. (a) Fig. (b) Fig. (c)

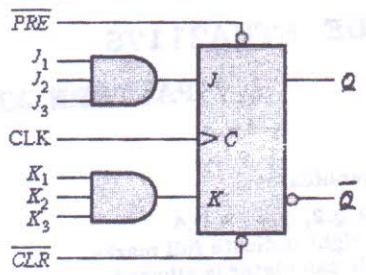
b) Design a 4-bit parallel data storage to store data 0110 using suitable flip-flop and explain it using waveforms **[6]**

c) Determine the Q waveform relative to the clock if the signals shown in figure are applied to the J-K flip-flop. Assume the Q is initially LOW. **[4]**



OR

Q2 a) The following serial data are applied to the flip-flop through the AND gates as indicated in figure. Determine the resulting serial data that appear on the Q output. There is one clock pulse for each bit time. Assume that Q is initially 0 and that PRE and CLR are HIGH. Rightmost bits are applied first. [6]
J1: 1 0 1 0 0 1 1; J2: 0 1 1 1 0 1 0; J3: 1 1 1 1 0 0 0;
K1: 0 0 0 1 1 1 0; K2: 1 1 0 1 1 0 0; K3: 1 0 1 0 1 0 1



b) What are the drawbacks of JK flip-flop? Explain working of Master-Slave JK flip-flop? [6]

c) Using D flip-flop design, divide clock frequency by 4 and explain its working with the help of waveforms [4]

Q3 a) Design a sequence generator to generate the sequence ...1011110... [6]

b) Design a 3 bit ring counter using suitable flip-flop, write its truth table and draw its waveform [4]

c) Design a MOD-6 Asynchronous counter using T flip-flops [4]

OR

Q4 a) For the data input and clock in shown in Fig. (a), determine the states of each flip-flop in the shift register of Fig. (b) and show the Q waveforms. Assume that the register contains all 1s initially. [6]

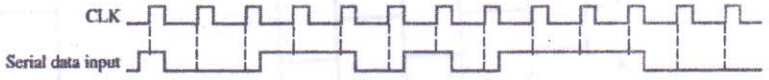


Fig. (a)

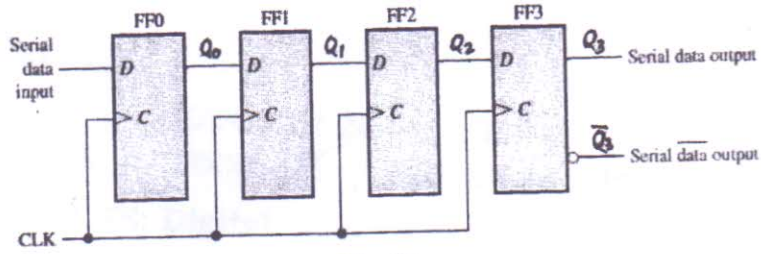


Fig. (b)

b) Design a synchronous counter to produce the following sequence. Use suitable flip-flop. 00, 10, 01, 11, 00,... **[4]**

c) Design a 3-bit Johnson counter using suitable flip-flop, write its truth table and draw its waveform **[4]**