Total No. of Questions – [04] Total No. of Printed Pages - [02]

G.R. No.	

OCTOBER 2018/ IN-SEM (T2) U218 – 145 (T2)

S. Y. B. TECH. (INFORMATION TECHNOLOGY) (SEMESTER - I)

COURSE NAME: DIGITAL ELECTRONICS AND LOGIC DESIGN

COURSE CODE: ITUA21175

(PATTERN 2017)

Time: [**1 Hour**] [Max. Marks: **30**]

(*) Instructions to candidates:

1) **Answer Q.1 OR Q.2 and Q.3 OR Q.4.**
2) **Figures to the right indicate full marks.**
3) **Use of scientific calculator is allowed**
4) **Use suitable data wherever required**

Q.1) a) Explain the operation of a twisted-ring counter and give its state diagram. [6 marks]

b) Design a Sequence Generator using Shift Register IC 74194 to generate the sequence 10110. [6 marks]

c) Convert JK flip-flop to D flip-flop. Show the design. [4 marks]

OR

Q.2) a) Design the circuit for 3-bit Synchronous Up-Counter. [6 marks]

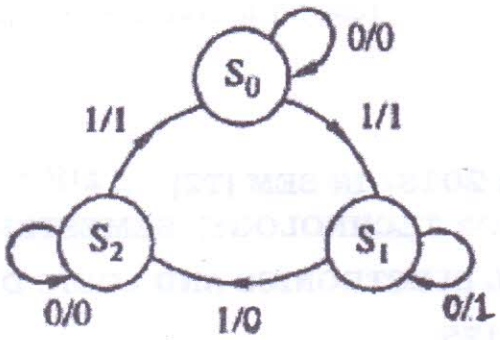
b) Design a divide-by-96 (MOD-96) counter using IC 7490. [6 marks]

c) Design the circuit for 3-bit Asynchronous Down-Counter. Show output waveforms of counter. [4 marks]

Q.3) a) Explain the basic architecture of FPGA with suitable diagram. [6 marks]

b) Design 4:1 MUX using suitable PAL. [4 marks]

c) Draw an equivalent ASM chart for the state diagram shown below. It has 3 states, inputs x, and outputs z. [4 marks]



OR

Q.4) a) Design 3-bit Binary to Gray code converter using suitable PLA. [6 marks]

b) Draw ASM chart for a 2 bit up counter with output 'Q1Q0' and Enable signal X is to be designed. If X=0, counter changes the state as '00-01-10-11'. If X=1, counter should remain in present state. [4 marks]

c) Explain the basic architecture of CPLD with suitable diagram. [4 marks]