

b) Calculation for MI

— 02 marks

Max^m stress $\tau = 137.6 \text{ N/mm}^2$ — 02 marks

c) $\tau = \frac{3}{2} \tau_{avg}$

OR

Q.4) a).

$M = 199 \text{ KN-m}$

$WL = 756$

$W = 369.2 \text{ KN}$

$L = 2.51 \text{ m}$

} 01 mark

} — 02 marks each

b) Shear force $AB = 0$, Bending moment $= W \cdot a$ } one mark each
SFD + BMD

c) at 40 mm $S = 144000 \text{ N}$, $\tau_{40} = 0$

at 20 mm $\tau_{20} = 33.76$ Fig-01

one mark each

*****Best Luck***

Marking Scheme

c) Design a Master-Slave Flip-Flop using J-K flip-flop.

[4]

1. Truth Table: 1 Mark

2. Logical Circuit Diagram: 3 Marks

Q3) a) Design a full adder circuit using PLA having three inputs, eight product terms, and two outputs.

[6]

1. Truth Table & Expression for Sum & Carry: 1 Marks

2. Kmaps & Expressions: 2 Marks

3. PLA Table: 1 Mark

4. Logical Circuit Diagram: 2 Marks

b) Implement a PLA for the given table

[4]

1. Logical Circuit Diagram: 4 Marks

c) Draw structural architecture of PLA & PAL.

[4]

1. PLA Structure: 2 Marks

2. PAL Structure: 2 Marks

OR

Q4) a) Implement $f_1(x_2, x_1) = \sum m(0,3)$, $f_2(x_2, x_1) = \overline{x_2 + x_1}$, and $f_3(x_2, x_1) = \prod M(1)$ with a 4 X 3 ROM.

[6]

1. Truth Table & Expression for Sum & Carry: 2 Marks

2. Logical Circuit Diagram: 4 Marks

b) What are types of PLD's? Draw structural diagram for any 3.

[4]

1. List of Type: 1 Mark

2. Structure of PLD: 3 Marks

c) Design ROM as PLD for 4 X 2 ROM.

[4]

1. Truth Table: 1 Mark

2. Logical Circuit Diagram: 3 Marks