G.R. No.

Paper Code-U219-1285 (BE-F&FS)

DECEMBER 2019/ENDSEM - Badelog Exam

S. Y. B. TECH. (COMPUTER ENGINEERING) (SEMESTER - I)

COURSE NAME:

DIGITAL SYSTEMS AND LOGIC DESIGN

COURSE CODE:

CSUA21175

(PATTERN 2017)

Time: [2 Hours]

[Max. Marks: 50]

Instructions to candidates:

- 1) Answer Q.1, Q.2, Q.3, Q.4, Q.5 OR Q.6, Q.7 OR Q.8
- 2) Figures to the right indicate full marks.
- 3) Use of scientific calculator is allowed
- 4) Use suitable data where ever required
- Q.1) a) Minimize the following function using K map and realize it with basic [6] gates.

 $F(A, B, C, D) = \sum m(0,1,2,5,8,10,11,14,15)$

OR

- b) Simplify the four variable Boolean function using Quine McCluskey Method. [6] $F(A, B, C, D) = \sum_{i=0}^{n} (0,1,2,3,5,7,8,10,12,13,15).$
- Q.2) a) Design 4-bit Excess-3 to BCD code converter. Use logic gates as per your [6] design and requirement.

OR

- b) Implement a 2 Bit Comparator along with truth table, k-map and logic [6] diagram using gates.
- Q.3) a) Design a divide by 96(MOD-96) counter using 7490 ICs. [6]

OR

b) Differentiate between synchronous and asynchronous counters along with [6] diagram.

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Q.4) a) Draw the architecture for PAL and PLA.	[4]
OR	
b) What are the applications of PLD's?	[4]
Q. 5) a) What is VHDL? Write VHDL code for structural model of full adder.	[6]
b) Draw an ASM chart to describe a mealy state machine that detects a sequence of 101 and that asserts a logical 1 at the output during the	[4]
last state of the sequence.	
c) What is ASM chart? Explain Mux Controller method using suitable example.	[4]
OR	
	26 (4)
Q.6) a) State the differences between concurrent and sequential statements of VHDL.	[6]
b) What are the advantages of VHDL.	[4]
c) Compare ASM & VHDL.	[4]
Q.7) a) Explain Arduino architecture in detail.	[6]
b) Write short note on soldiering techniques?	[4]
c) What is the classification of logic families?	[4]
OR	
Q.8) a) Explain the parameter to characterize logic families.	[6]
b) What are the applications of Raspberry pi?	[4]
c) Explain CMOS and RTL?	[4]
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