Total No. of Questions – [ 08 ] Total No. of Printed Pages 03

| G.R. No. | |
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paper code: U219-136 (BE-F & FS)

**DECEMBER 2019/ENDSEM** Backlog Exam

## S. Y. B. TECH. (E&TC) (SEMESTER - I)

## COURSE NAME: DIGITAL ELECTRONICS

## COURSE CODE: ETUA21175

**(PATTERN 2017)**

Time: [**2 Hours**] [Max. Marks: **50**]

**(*) Instructions to candidates:**

1) **Answer Q.1, Q.2, Q.3, Q.4, Q.5 OR Q.6, Q.7 OR Q.8**
2) **Figures to the right indicate full marks.**
3) **Use of scientific calculator is allowed**
4) **Use suitable data where ever required**

Q 1) a) Minimize the given expression using K-map **[6]**

$Y = \bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{D} + AB\bar{C}\bar{D} + \bar{A}\bar{B}CD + A\bar{B}CD + \bar{A}\bar{B}C\bar{D} + \bar{A}BC\bar{D} + ABC\bar{D} + A\bar{B}C\bar{D}$

**OR**

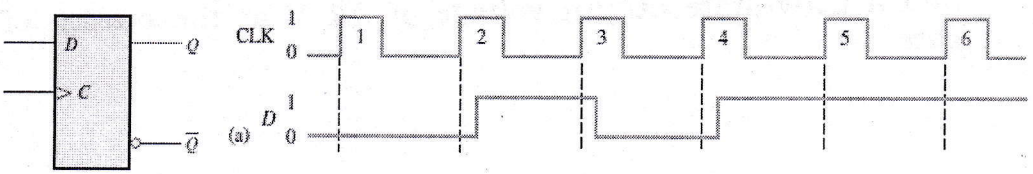
b) A four variable function is given as f(A,B,C,D) = Σm(0,2,3,4,5,7,9,13,15). Use a K-map to minimize the function. **[6]**

Q 2) a) Design a logic circuit that will compare two 2-bit numbers and produce output A>B, A=B, A<B. Write the truth table and draw its logic diagram. **[6]**

**OR**

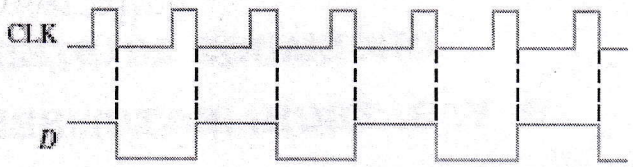
b) Develop a logic circuit with four input variables that will only produce a 1 output when exactly three input variables are 1s. **[6]**

Q 3) a) Determine the Q and $\bar{Q}$ output waveforms of the flip-flop D and CLK inputs shown in Figure. Assume the positive edge triggered flip-flop is initially reset. **[6]**




**OR**

b) Determine the Q and $\overline{Q}$ output waveforms of the flip-flop D and CLK inputs shown in Figure. Assume the negative edge triggered flip-flop is initially reset. **[6]**




Q 4) a) Design a sequential circuit which will follow the sequence 000, 001, 010, 011, 100, 101, 000... using suitable flip-flop and draw its logic diagram. **[4]**

**OR**

b) A system packs half dozen of oranges in a box. Design a system which will count the number of oranges until the box is filled and then restart the count from zero for filling of next box. Design the system using suitable flip-flops and draw its logic diagram. **[4]**

Q 5) a) A certain TTL IC has four two input NAND gates. Draw the internal structure of single NAND gate and explain its working for all the possible input combinations. **[6]**

b) Draw the block diagram of generic FPGA architecture, and write its parameters. **[4]**

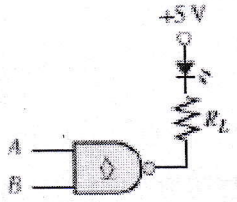
c) When a standard TTL NAND gate drives five TTL inputs, how much current does the driver output source, and how much does it sink? **[4]**
Source current in HIGH output state: $I_{IH}$(max) = 40 μA per input
Sink current in LOW output state: $I_{IL}$(max) = -1.6mA per input

**OR**

Q 6) a) A certain CMOS IC has four two input NAND gates. Draw the internal structure of single NAND gate and explain its working for all the possible input combinations. **[6]**

b) Draw the generic architecture of CPLD and write its parameters. **[4]**

c) Determine the value of the limiting resistor, $R_L$, in the open-collector circuit of figure if the LED current is to be 20 mA. Assume a 1.5 V drop across the LED when it is forward-biased and a LOW-state output voltage of 0.1 V at the output of the gate. **[4]**




Q 7) a) A long sequences of pulses enters a synchronous sequential circuit which is required to produce an output z=1, whenever the sequence 1001 occurs. Design the non-overlapping system and draw its logic diagram. **[6]**

b) With suitable example explain the following terms: **[4]**
1. State Table 2. State diagram

c) Write truth table, excitation table for D flip-flop and draw its state diagram. **[4]**

**OR**

Q 8) a) A long sequences of pulses enters a synchronous sequential circuit which is required to produce an output z=1, whenever the sequence 1010 occurs. Design the non-overlapping system and draw its logic diagram. **[6]**

b) Write truth table, excitation table for JK flip-flop and draw its state diagram. **[4]**

c) Design a sequence detector which will produce output z=1, whenever the sequence 111 occurs. **[4]**