Total No. of Questions – [08] Total No. of Printed Pages [02]

G.R. No.	

Paper code -U229-145 (BE-F&FS)

DEC 2019/ENDSEM - Backlog Exam

S. Y. B. TECH. (IT) (SEMESTER - II)

COURSE NAME: COMPUTER ORGANIZATION & MICROPROCESSOR

COURSE CODE: ITUA22175

(PATTERN 2017)

Time: [2 Hours] [Max. Marks: 50]

(*) Instructions to candidates:

1) **Answer Q.1, Q.2, Q.3, Q.4, Q.5 OR Q.6, Q.7 OR Q.8**
2) **Figures to the right indicate full marks.**
3) **Use of scientific calculator is allowed**
4) **Use suitable data wherever required**

Q.1) a) Digramatically represent the computer architecture and explain it. [6]

OR

b) Explain the computer functions in detail, with digram. [6]

Q. 2) a) Explain any one method for multiplication of positive numbers with example. [6]

OR

b) Deatil the functioning of Arithmetic and Logic Unit.

Q.3) a) Draw and explain the elements of program execution in detail. [6]

OR

b) Explain any one design Issues. [6]

Q.4) a) Describe any tew addressing modes with example. [4]

OR

b) Write about register organization in processor. [4]

Q. 5 a) Draw and explain elements of cache design. [6]

b) Discuss any two performance characteristics of two level cache. [4]

c) List out the elements of cache design and explain any one in brief. [4]

OR

Q.6) a) List out and discuss performance characteristics of two level cache. [6]

b) Explain the impact of cache design parameter -cache size on processor's performance and list out other cache design parameters. [4]

c) Discuss the elements affecting on cache performance. [4]

Q.7) a) Describe multicore organizations in detail. [6]

b) Compare simple instruction pipelining and superscalar approach. [4]

c) What is SMT approach? How does it enhance the performance? [4]

OR

Q.8) a) Describe Intel Core i7 multicore organizations in detail. [6]

b) Compare superscalar and simultaneous Multithreading. [4]

c) What are the hardware performance issues, discuss in brief.. [4]