Total No. of Questions – [06] Total No. of Printed Pages: [02]

G.R. No.	

paper code comp: U239-121 (ESE)
IT : U239-141 (ESE)

DECEMBER 2019 ENDSEM
S. Y. B.TECH. (COMPUTER ENGINEERING/INFORMATION TECHNOLOGY)
(SEMESTER –III)
COURSE NAME: ANALOG AND DIGITAL ELECTRONICS
COURSE CODE: CSUA21181/ITUA21181
(PATTERN 2018)

Time: [2 Hours] [Max. Marks: 50]

Instructions to candidates:
1) All questions are compulsory.
2) Figures to the right indicate full marks.
3) Use of scientific calculator is allowed.
4) Assume suitable data where ever required.

Q.1) Attempt any **one**

a) Convert decimal number (1102) into hexadecimal number and Octal number (0.3467) into hexadecimal number. [4]

b) Simplify the Boolean algebraic expression for designing digital circuits using K-Map: [4]

$$F(A, B, C, D) = \sum m (0,1,2,5,8,10,11,14,15)$$

Q.2) Attempt any **one**

a) Obtain 16:1 MUX using 4:1 MUX.
Obtain 1:8 DEMUX using two 1:4 DEMUX. [4]

b) Explain Parity Generator and Checker. [4]

Q.3) Attempt any **one**

a) Explain Race around condition in J-K flip flop and How it is eliminated in Master Slave J-K flip flop. [6]

b) Explain working of Shift registers (SISO, SIPO, PIPO) with diagrams. [6]

Q.4) Attempt any **one**

a) Design a 3-bit Synchronous UP/DOWN counter using J-K flip-flops and differentiate between Moore and Mealy models. [10]

b) Design MOD 99 Counter using IC 7490 and sequence detector for the sequence 101 using Moore machine. [10]

Q.5) Attempt any **one**

a) Explain standard TTL characteristics and operation of TTL NAND gate with example. [13]

b) Explain Arduino architecture and soldiering techniques for mounting of devices on PCB [13]

Q.6) Attempt any **one**

a) Draw block diagram of PLD and Implement the combinational circuit with a PLA having 3 inputs, 4 product terms and 2 outputs for the function: [13]

F1(A, B, C) = ∑m (0,1,2,4)

F2(A, B, C) = ∑m (0,5,6,7)

b) Explain VHDL Modeling Styles and write a VHDL code using Structural, Dataflow, and Behavioral model by considering Half Adder as entity. [13]