Total No. of Questions – [06]

Total No. of Printed Pages: 02

G.R. No.	

Paper code – U239-135 (ESE)

DECEMBER 2019 ENDSEM

S. Y. B.TECH. (Electronics & Telecommunication) (SEMESTER – III)

COURSE NAME: Digital System Design

COURSE CODE: ETUA21185

(PATTERN 2018)

Time: [2 Hours] [Max. Marks: 50]

(*) Instructions to candidates:

1) All questions are compulsory.
2) Figures to the right indicate full marks.
3) Use of scientific calculator is allowed.
4) Assume suitable data where ever required.

Q.1) Attempt any **one**

a) Using K-map, simplify and obtain minimized SOP expression and draw its logic diagram [4]

$$Y = \Sigma m(0,1,2,14,15) + d(3,5,7)$$
$$Y = \Sigma m\,(0,1,2,3,8,9,10,11) + d(6,14)$$

b) Using K-map, simplify and obtain minimized POS expression and draw its logic diagram [4]

$$Y = (\bar{A}+\bar{B}+C+D)(\bar{A}+\bar{B}+C+\bar{D})(A+B+\bar{C}+\bar{D})(\bar{A}+B+C+\bar{D})(A+\bar{B}+\bar{C}+\bar{D})$$

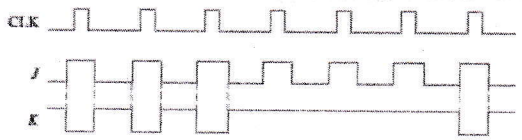
Q.2) Attempt any **one**

a) Design a logic circuit which will subtract three numbers of one bit each and gives output as difference and borrow, draw its logic diagram. [4]

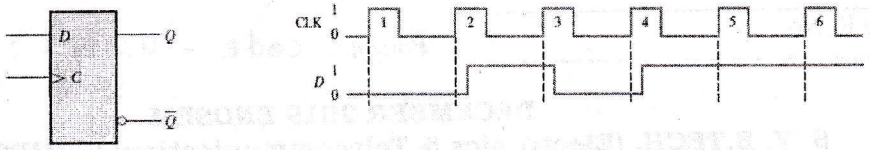
b) Design 3-bit gray to binary code converter and draw its logic diagram. [4]

Q.3) Attempt any **one**

a) Determine the Q output waveforms of the flip-flop JK and CLK inputs shown in Figure. Assume the negative edge triggered flip-flop is initially reset. [6]



b) Determine the Q and $\overline{Q}$ output waveforms of the flip-flop D and CLK inputs shown in Figure. Assume the positive edge triggered flip-flop is initially reset. [6]



Q.4) Attempt any **one**

a) Using D flip-flop design a Asynchronous three bit down counter. Write truth table and draw its logic diagram. [10]
Design MOD-6 synchronous up counter using D flip flop. Write its truth table and draw its logic diagram.

b) Using D flip-flop design a Synchronous four bit up-counter, Draw its logic diagram. [10]
Design MOD-6 synchronous down counter using D flip flop. Write its truth table and draw its logic diagram.

Q.5) Attempt any **one**

a) A certain TTL IC has six one input NOT gates. Draw the internal structure of single NOT gate and explain its working for all the possible input combinations. [13]
Draw the block diagram of generic CPLD architecture, and write its parameters.

b) A certain CMOS IC has four two input NOR gates. Draw the internal structure of single NOR gate and explain its working for all the possible input combinations. [13]
Draw the generic architecture of FPGA and write its parameters.

Q.6) Attempt any **one**

a) List the modeling style of VHDL? Explain data flow modeling with suitable example? Write Syntax for When-Else? [13]
Write VHDL code for JK flip-flop?

b) List the modeling style of VHDL? Explain Behavioral modeling in VHDL with suitable example? Write syntax for if-then-else in VHDL? [13]
Write VHDL code for half adder?