Total No. of Questions – [06] Total No. of Printed Pages: [03]

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Paper Code – U 239-134 (ESE)

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S. Y. B.TECH. (E & TC) (SEMESTER –III)

COURSE NAME: Electronics Devices & Circuits
COURSE CODE: ETUA21184

(PATTERN 2018)

Time: [2 Hours] [Max. Marks: 50]

(*) Instructions to candidates:
1) All questions are compulsory.
2) Figures to the right indicate full marks.
3) Use of scientific calculator is allowed.
4) Assume suitable data where ever required.

Q.1) Attempt any **one**

a) Compare Full wave and half wave rectifier with neat diagrams of both and other parameters. [4]

b) Explain working principle of LED and state its applications. [4]

Q.2) Attempt any **one**

a) Voltage divider biasing circuit uses silicon BJT has $\beta = 150$, $V_{CC} = 5$ V, $R_1 = 9$ KΩ, $R_2 = 2.25$ KΩ, $R_E = 200$ Ω and $R_c = 1$ KΩ. Find I_{BQ}, and I_{CQ}. [4]

b) Draw and explain hybrid model of BJT for common emitter configuration. [4]

Q.3) Attempt any **one**

a) The self-bias circuit using n-channel JFET has $V_{DD} = 18$ V, $R_D = 4.7$ KΩ, $R_S = 1.5$ KΩ and $R_G = 1$MΩ. Determine the co-ordinates of Q point such as I_{DQ}, V_{GSQ} and V_{DSQ}. Assume JFET has $V_P = -4$V, $I_{DSS} = 8$ mA and $g_m = 5$ mS. [6]

b) CS amplifier using n-channel JFET with self-bias and unbypassed source resistor has $R_G = 1.5$ MΩ, $R_D = 3$ KΩ, $R_S = 1.2$ KΩ, and $V_{DD} = 20$ V. The JFET parameters are $I_{DSS} = 8$ mA, $V_P = -8$ V and $Y_{OS} = 20$ µS, $V_{GSQ} = -2$ V, $I_{DQ} = 2$ mA. Calculate g_m, r_o and Av. [6]

Q.4) Attempt any **one**

a) Voltage divider biasing circuit using n-channel E-MOSFET has $V_{DD} = 5$V, $R_1 = 30$ KΩ, $R_2 = 20$ KΩ, $R_D = 20$KΩ, $V_T = 1$V, $K_n = 0.1$ mA/v². Determine the co-ordinates of Q point such as V_{DSQ}, V_{GSQ} and I_{DQ}. [6+4]

Explain following non-ideal effects for MOSFET.
i) Break down effect
ii) Channel length modulation.

b) Draw the constructional (structure) diagram of n-channel E-MOSFET and explain its working with the help of both characteristics. [6+4]

An NMOS transistor is fabricated in a 0.4-μm process having μnCox = 200 μA/V2 and VA = 40 V. If L = 0.8 μm and W = 16 μm. Find λ and ID that results when the device is operated with an overdrive voltage (VGS - VT) = 0.5 V and VDS = 1 V.

Q.5) Attempt any **one**

a) Common source amplifier using n-channel E-MOSFET has R_1 = 40 MΩ, R_2 = 10 MΩ, R_D = 4.7 KΩ, R_{sig} or R_{Source} = 2.2 KΩ and V_{DD} = 25 V. If MOSFET parameters are V_T = 3 V, K_n = 0.4 mA/V² and ro = 40 KΩ. Calculate Av, Ri and Ro. [7+6]

Draw voltage divider biasing common source amplifier circuit using n-channel E-MOSFET and write the expressions for AV, Ri and Ro.

b) Determine I_{DQ}, gm and ro for a MOSFET CS amplifier if V_{DD} = 5V, V_{GSQ} = 2.12V, R_D = 2.5KΩ. Assume transistor parameters as V_T = 1V, K_n = 0.8 mA/V² and λ =0.02/V. [7+6]

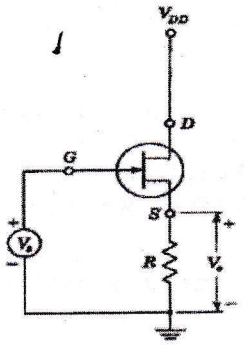
Draw and explain the high frequency AC equivalent circuit for n channel E-MOSFET and explain the effect of source terminal resistances, Rs on the gain of the CS amplifier.

Q.6) Attempt any **one**

a) Explain working of Hartley oscillator with neat circuit diagram. A Hartley Oscillator circuit has two inductances of L1=L2 =100 μH and C = 0.05μF. Determine the frequency of oscillations of the circuit. [7]

Draw block schematic of following feedback topologies:
i) Voltage shunt feedback topology
ii) Current shunt feedback topology
iii) Current series feedback topology

b) For the FET source follower circuit, calculate values of Avf, R_{if}, R_{of} and R'_{of}. Assume g_m = 2 mA/V and r_d = 40 KΩ and R= 3KΩ. [7+6]



Draw the block diagram of voltage series negative feedback amplifier and derive the expression for Avf.