G.R. No.	

Paper Code – U 239-144 (ESE)

DECEMBER 2019 ENDSEM
S. Y. B.TECH. (IT) (SEMESTER – III)
COURSE NAME: COMPUTER ORGANIZATION
COURSE CODE: ITUA21184
(PATTERN 2018)

Time: [2 Hours]   [Max. Marks: 50]

(*) Instructions to candidates:
1) All questions are compulsory.
2) Figures to the right indicate full marks.
3) Use of scientific calculator is allowed.
4) Assume suitable data where ever required.

Q.1) **Attempt any one**
   a) Point out and discuss techniques which contribute to microprocessor speed.   [4]
   b) Explain functionality of Control lines, address lines and data lines in bus interconnection scheme.   [4]

Q.2) **Attempt any one**
   a) Solve 10100.01 – 11011.10 using 2's Complement method.   [4]
   b) Explain IEEE 754 floating point number format representation for single precision and Double precision format. [4]

Q.3) **Attempt any one**
   a) Write about concept of register renaming along with its hazards.   [6]
   b) Summarize on hardwired control unit organization along with list of components required to design.   [6]

Q.4) **Attempt any one**
   a) Draw and explain 8086 block diagram architecture along with suitable diagram.   [10]
      Write on Direct addressing mode with suitable example.

   b) Correlate the following instruction with type of Involved along with its description.   [10]
      LD,STC,LR,INC,MOV,Input(read)

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Explain Logical address, Physical address and Effective Address with suitable example.

Q.5)   **Attempt any one**
   a)   Discuss about cache memory. Compare physical cache and logical cache with suitable diagram. Select which one more better in terms of speed.   [13]
        Discuss on memory hierarchy with suitable diagram.

   b)   Write cache read operation flowchart in detail and summarize the same.   [13]
        Choose the appropriate parameters which affect memory Performance.

Q.6)   **Attempt any one**
   a)   Comment on single core, dual core, quad core and multicore processors. Which one is a better processor along with application of each. Also compile the same to write about hardware performance issues and software performance issues.   [13]

   b)   List four types of multicore organization with suitable Diagram and Explain role of L1, L2 and L3 Cache.   [13]
        What is Interrupt? Enumerate different sources of interrupt along with states of interrupt.

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