Total No. of Questions – [08] Total No. of Printed Pages: 04

G.R. No.	

Paper Code - U218-134 (CBE-FS)

MAY 2019/ENDSEM

S. Y. B. TECH. (E&TC) (SEMESTER - I)

COURSE NAME: Semiconductor Devices & Circuits

COURSE CODE: ETUA21174

(PATTERN 2017)

Time: [**2Hours**] [Max. Marks: **50**]

(*) Instructions to candidates:

1) **Answer Q.1, Q.2, Q.3, Q.4, Q.5 OR Q.6, Q.7 OR Q.8**
2) **Figures to the right indicate full marks.**
3) **Use of scientific calculator is allowed**
4) **Use suitable data whereever required**

Q.1) a) Voltage divider circuit uses silicon transistor with β=50, V_{cc}=20V and R_c=5KΩ.It is desired to establish a Q point at V_{CE}=11.5V, I_c=1.5mA and stability factor =3. Determine R_E, R_1 and R_2. [6 marks]

OR

b) Draw Hybrid equivalent model using transistor for CE configuration and write the significance of each parameter. [6 marks]

Q. 2)a) The self-bias circuit using n-channel JFET has V_{DD}=18V, R_D=4.7KΩ,R_S=1.5KΩ and R_G=1MΩ.Determine the co-ordinates of Q point such as I_{DQ}, V_{GSQ} and V_{DSQ}. Assume JFET has V_P= 4V, I_{DSS}= 8mA and g_m= 5mS. [6 marks]

OR

b) Explain with neat circuit diagram the self biasing circuit for n-channel JFET [6 marks]

Q. 3) a) Voltage divider biasing circuit using n-channel MOSFET has V_{DD} = 40V, R_1=22 MΩ, R_2= 18 MΩ,R_D=3KΩ,R_S=820 Ω, V_{TH}=5V, $I_{D(ON)}$=3 mA and $V_{GS(ON)}$=10 V. Determine the co-ordinates of Q point such as V_{DSQ}, V_{GSQ}, and I_{DQ}. [6 marks]

OR

b) Explain the working principle of n-channel enhancement MOSFET along with its constructional diagram. [6 marks]

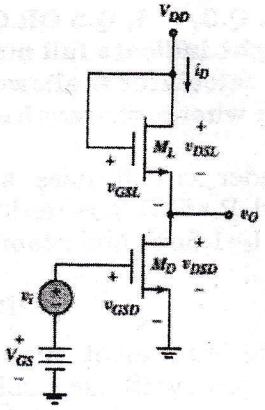
[4 marks]

Q. 4) a) Draw complete AC equivalent model for n-channel MOSFET CS amplifier with bypass capacitor and without bypass capacitor. Write small-signal voltage gain expression for both CS amplifiers.

OR

b) For CS amplifier using MOSFET determine g_m, I_D and r_o if V_T= 1 V, K_n= 0.8 mA/V², λ= 0.01 /V, V_{GSQ}= 3V. [4 marks]

Q. 5) a) Design an NMOS amplifier with an enhancement load shown in figure to provide a small-signal voltage gain of |Av| = 10. The Q-point is to be in the center of the saturation region. Determine V_{GSQ} and V_{DSQ} of driver transistor. The circuit is to be biased at V_{DD}= 5 V. NMOS transistors with parameters V_{TN}= 1 V, k'_n= 60 µA/V², and λ = 0 are available. The minimum width-to-length ratio $(W/L)_{min}$ is = 2. [6 marks]

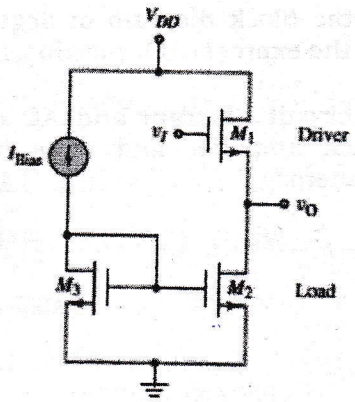


b) Draw MOSFET as a practical switch model. Explain the significance of each component. [4 marks]

c) Draw current source circuits. Explain how to improve its output resistance. [4 marks]

OR

Q. 6)a) The transconductance g_{m1} of the transistor M_1 in the circuit of figure is to be changed by changing the bias current such that the output resistance of the circuit is R_o= 2 kΩ. Assume the bias voltage is V_{DD}= 3.3 V. Assume that all transistors are matched with parameters V_{TN}= 0.4 V, K_n= 0.20 mA/V², and λ = 0.01 V^{-1}. The drain current in M_1 is I_{D1} = I_{Bias} = 0.2 mA. (a) What are the required value of g_{m1} and new value of I_{Bias}? (b) Using the results of part (a), what is the small-signal voltage gain? [6 marks]



b) Sketch CMOS common-gate amplifier circuit and its small-signal equivalent circuit. Write expression for small-signal voltage gain and output resistance. [4 marks]

c) Explain with neat diagram the working principle of current mirror circuit? [4 marks]

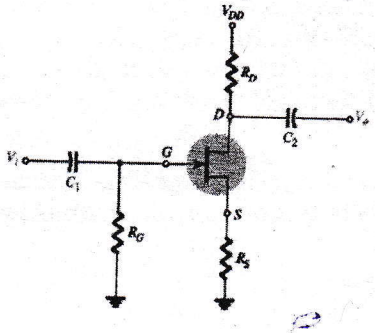
Q. 7) a) Draw block schematic of following feedback topologies:
i) Voltage series feedback topology
ii) Current shunt feedback topology
[6 marks]

b) Explain Barkhausen criteria to obtain sustained oscillations at the output. [4 marks]

c) Explain Hartley oscillator with neat circuit diagram. Also writeit's cut off frequency expression. [4 marks]

OR

Q. 8) a) For current series feedback amplifier, determine G_{mf}, A_{vf}, R_{if}, R'_{of} if R_s=1KΩ, R_D= 5 KΩ, R_G=1MΩ, g_m=2mA/V and r_o=20KΩ. [6 marks]



b) Draw the block diagram of negative feedback amplifier and derive the expression for feedback gain A_{vf}. [6 marks]

c) Draw circuit diagram and AC equivalent of voltage series feedback amplifier and write it's final expression for ac parameters. [4 marks]