Total No. of Questions – [08] Total No. of Printed Pages 03

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Paper Code - U218-135(BE-FF)

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S. Y. B. TECH. (E&TC) (SEMESTER - I)

COURSE NAME: DIGITAL ELECTRONICS

COURSE CODE: ETUA21175

(PATTERN 2017)

Time: [**2 Hours**] [Max. Marks: **50**]

(*) Instructions to candidates:

1) **Answer Q.1, Q.2, Q.3, Q.4, Q.5 OR Q.6, Q.7 OR Q.8**
2) **Figures to the right indicate full marks.**
3) **Use of scientific calculator is allowed**
4) **Use suitable data where ever required**

Q 1) a) A four variable function is given by, F (A,B,C,D)= Σm(2,9,10,12,13)+D(15,14). Use k-map to minimize the function in SOP. **[6]**

OR

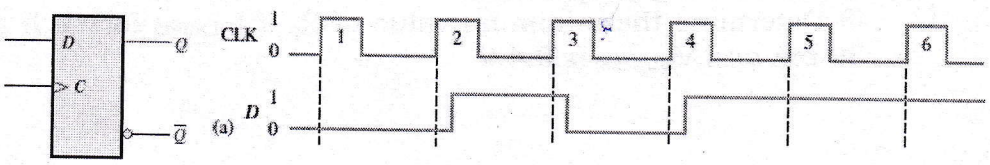
b) A four variable function is given as f(A,B,C,D) = Σm(0,2,3,4,5,7,9,13,15). Use a K-map to minimize the function in SOP. **[6]**

Q 2) a) A certain telephone exchange uses multiplexers for routing calls from its exchange to another. Design a multiplexer having capacity of eight inputs and single output which routes only odd number of inputs. **[6]**

OR

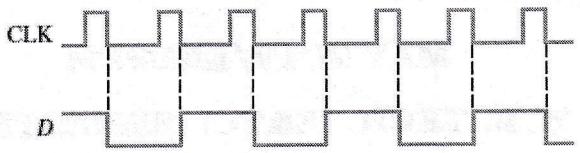
b) Develop a combinational system which has three input and produces output Y. Whenever even number of ones are detected by the system Output Y=1. Write the truth table and draw its logic diagram. **[6]**

Q 3) a) Determine the Q and $\overline{Q}$ output waveforms of the flip-flop D and CLK inputs shown in Figure. Assume the positive edge triggered flip-flop is initially reset. **[6]**



OR

b) Draw the Q output relative to the clock for a D flip-flop with the inputs as shown in fig. Assume positive edge triggering and Q initially LOW. **[6]**



Q 4) a) Design a sequential circuit which will follow the sequence 000, 001, 010, 011, 100, 101, 000... using suitable flip-flop and draw its logic diagram. **[4]**

OR

b) Design a synchronous circuit using suitable flip-flop which will follow the sequence 00, 01, 10, 11, 00... write its truth table and draw its logic diagram. **[4]**

Q 5) a) A certain CMOS IC has four two input NAND gates. Draw the internal structure of single NAND gate and explain its working for all the possible input combinations. **[6]**

b) Draw the block diagram of generic FPGA architecture, and write its parameters. **[4]**

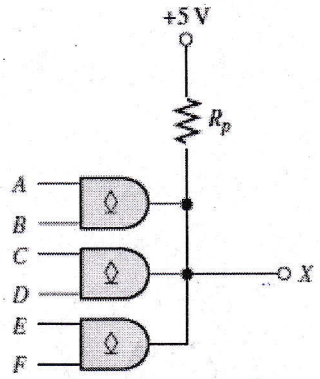
c) Determine the High-level and Low-level noise margins for CMOS and for TTL. **[4]**
For 5V CMOS, VIH(min) = 3.5 V , VIL(max) = 1.5 V,
VOH(min) = 4.4 V ,VOL(max) = 0.33 V.
For 5V TTL, VIH(min) = 2 V ,VIL(max) = 0.8 V ,
VOH(min) = 2.4 V ,VOL(max) = 0.4 V

OR

Q 6) a) A certain TTL IC has four two input NAND gates. Draw the internal structure of single NAND gate and explain its working for all the possible input combinations. **[6]**

b) A certain CMOS IC is of NOT gate. Draw the internal structure of CMOS NOT gate and explain the working for all the possible input combination. **[4]**

c) Three open-collector AND gate are connected in a wired AND configuration as shown in figure. Assume that the wired-AND circuit is driving four standard TTL inputs (-1.6 mA each). **[4]**
i) Write the logic expression for X.
ii) Determine the minimum value of R_p if $I_{OL(max)}$ for each gate is 30 mA and $V_{OL(max)}$ is 0.4 V



Q 7) a) A long sequences of pulses enters a synchronous sequential circuit which is required to produce an output z=1, whenever the sequence 1111 occurs. Design the non-overlapping system and draw its logic diagram. **[6]**

b) Design a sequence detector which will produce output z=1, whenever the sequence 101 occurs. **[4]**

c) Write truth table, excitation table for SR flip-flop and draw its state diagram. **[4]**

OR

Q 8) a) A long sequences of pulses enters a synchronous sequential circuit which is required to produce an output z=1, whenever the sequence 1111 occurs. Design the non-overlapping system and draw its logic diagram. **[6]**

b) Write truth table, excitation table for JK flip-flop and draw its state diagram. **[4]**

c) With suitable example explain the following terms: **[4]**
1. State Table 2. State diagram