Total No. of Questions – [08] Total No. of Printed Pages [02]

G.R. No.	

Paper code - U218-145 (BE-FF)

MAY 2019/ENDSEM

S. Y. B. TECH. (INFORMATION TECHNOLOGY) (SEMESTER - I)

COURSE NAME: DIGITAL ELECTRONICS AND LOGIC DESIGN

COURSE CODE: ITUA21175

(PATTERN 2017)

Time: [**2 Hours**] [Max. Marks: **50**]

(*) Instructions to candidates:

1) **Answer Q.1, Q.2, Q.3, Q.4, Q.5 OR Q.6, Q.7 OR Q.8**
2) **Figures to the right indicate full marks.**
3) **Use of scientific calculator is allowed**
4) **Use suitable data where ever required**

Q.1) a) Write Binary, BCD, Excess-3, and Gray code for decimal number 27. Show all the steps in conversion. [6 marks]

OR

b) Perform following arithmetic using 2's Complement : [6 marks]

i) $(6)_{10} - (10)_{10}$

ii) $(-6)_{10} - (10)_{10}$

iii) $(-6)_{10} + (10)_{10}$

Q.2) a) List rules of Excess-3 addition with example. Design (Truth Table, K-map, Logic Function, Circuit Diagram) Excess-3 Adder using IC 7483. [6 marks]

OR

b) Explain 3:8 Decoder IC 74138. Design (Truth Table, Logic Function, Circuit Diagram) Full Adder using IC 74138. [6 marks]

Q.3) a) Draw pin diagram of IC 74191 & state function table. Design & draw Mod-11 (5 to 15) truncated UP counter using IC 74191. [6 marks]

OR

b) Convert (Truth Table, K-map, Logic Function, Circuit Diagram) JK flip-flop to D flip-flop. Show the design. [6 marks]

Q.4) a) Implement the following functions using PLA [4 marks]

$A(P, Q, R) = \sum m (0, 1, 6, 7)$

$B(P, Q, R) = \sum m (1, 2, 4, 6)$

OR

b) Compare: [4 marks]

i) PAL and PLA

ii) FPGA and CPLD

Q.5) a) List and explain the different VHDL program modeling styles. [6 marks]

b) What is the difference between Sequential and Concurrent execution of VHDL statements? [4 marks]

c) Declare entity and architecture for 4:1 MUX VHDL module. [4 marks]

OR

Q.6) a) What is VHDL? Write features of VHDL. Explain the structure of VHDL module. [6 marks]

b) List any 4 operators used in VHDL code and explain each with example. [4 marks]

c) Declare entity and architecture for 3:8 Decoder VHDL module. [4 marks]

Q.7) a) Explain Flag Registers of 8086 Microprocessor. [6 marks]

b) List main features of 8051 Microcontroller. [4 marks]

c) Explain the Von Neumann architecture with neat diagram. [4 marks]

OR

Q.8) a) Draw 8086 architecture and explain each functional block. [6 marks]

b) Draw and explain the Harvard architecture. [4 marks]

c) Compare Microprocessor and Microcontroller with their applications. [4 marks]