Total No. of Questions – [08] Total No. of Printed Pages: [02]

G.R. No.	

Paper code - U228 - 134 (ESE)

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S. Y. B. TECH. (E & TC) (SEMESTER - II)

COURSE NAME: Integrated Circuits (IC)

COURSE CODE: ETUA22174

(PATTERN 2017)

Time: [**2 Hours**] [Max. Marks: **50**]

(*) Instructions to candidates:

1) **Answer Q.1, Q.2, Q.3, Q.4, Q.5 OR Q.6, Q.7 OR Q.8**
2) **Figures to the right indicate full marks.**
3) **Use of scientific calculator is allowed**
4) **Use suitable data wherever required**

Q1 **a)** Draw the circuit diagram of Dual input balanced output differential amplifier and derive the expressions for differential voltage gain (Ad), Input resistance (Rin)and output resistance (Ro) using r parameter model. **[6]**

OR

b) Op-amp has slew rate of 2 V/microsecond. What is the frequency of maximum undistorted sine wave that can be obtained for 5 V peak signal? Also determine the maximum current which charges the internal capacitor of 1 nano farad. **[6]**

Q2 **a)** What are the drawbacks of ideal/basic integrator? Draw the circuit diagram of practical integrator along with frequency response and explain its operation. **[6]**

OR

b) For practical differentiator the component values are R_1=12 K ohm, R_f =120 K ohm and capacitor C_1 = 10 nano farad. C_f = 1 nano farad **[6]**

1. draw the circuit diagram
2. determine the differentiator frequency, f_a
3. Determine the dc gain

Q3 **a)** Draw circuit diagram of precision full wave rectifier. Draw input and output waveforms. Explain with necessary equations, how the circuit provides full wave rectification ? **[6]**

OR

b) Draw circuit diagram of negative peak detector. Describe its working with neat waveforms. What changes need to be **[6]**

incorporated in the circuit for detecting the positive peak voltage? Draw the modified circuit.

Q4 a) Draw circuit diagram of second order Butterworth low pass filter and describe its frequency response with the help of gain equation. [4]

OR

b) Determine the cut off frequency of first order Butterworth high pass filter if R = 1k ohm and C = 0.1 micro farad. Determine the gain of circuit at 1.59 KHz and 1 KHz. R_1= 1 K ohm and R_f = 2 K ohm. [4]

Q5 a) Draw the schematic diagram of 3 bit Successive Approximation (SAR) type ADC. Describe how the circuit works and explain how it gives binary code $(1\ 0\ 0)_2$ for analog input 4 V. Consider analog input range between 0 to 8 V. [6]

b) Compare Binary weighted type D to A converter with R-2R ladder type DAC. [4]

c) State any two parameters of ADC. An 8 bit SAR type ADC is driven by a clock of 1 MHz. Determine the conversion time required. [4]

OR

Q6 a) Draw the circuit diagram of R – 2R ladder type DAC. Describe how the circuit converts the code $(0\ 0\ 1)_2$ to 1/8 volts. [6]

b) What is the resolution of D to A converter? A 10 bit DAC has reference voltage/ full scale voltage 10.23 V. Determine its resolution/step size. [4]

c) Draw the circuit diagram of grounded load V to I converter and describe its operation. Draw its transfer characteristics. [4]

Q7 a) Give any two parameters of PLL and describe them with respect to transfer characteristics of PLL. Draw schematic diagram of IC 565. [6]

b) Draw block diagram of PLL and Describe function of each block. [4]

c) Draw block diagram for PLL to obtain $f_{out} = 10\ f_{in}$ and describe it's working. [4]

OR

Q8 a) Draw the transfer characteristics of PLL and describe its working with its different modes of operation. [6]

b) Draw schematic diagram of IC 565. In PLL IC 565 determine free running frequency, lock range and capture range. Given demodulation capacitor C = 1 micro Farad, Resistor and capacitor of VCO, R_1 = 15 k ohms and C_1 = 0.01 micro farad. Vcc = 12 V and –Vcc = 0 V (gnd). [4]

c) Describe how PLL is used as FM demodulator? [4]