G.R. No. |

Paper code- U228-145 (ESE)

MAY 2019/ENDSEM

S. Y. B. TECH. (IT) (SEMESTER - II)

COURSE NAME: Computer Organization & Microprocessor
COURSE CODE: ITUA22175

(PATTERN 2017)

Time: [2 Hours]   [Max. Marks: 50]

(*) Instructions to candidates:
1) Answer Q.1, Q.2, Q.3, Q.4, Q.5 OR Q.6, Q.7 OR Q.8
2) Figures to the right indicate full marks.
3) Use of scientific calculator is allowed
4) Use suitable data wherever required

Q.1) a) Explain IAS(Von Neumann) architecture with the help of neat diagram   [6]

OR

b) Explain basic instruction cycle with neat diagram and example   [6]

Q.2) a) Explain booth's algorithm   [6]

OR

b) Using Booth's algorithm multiply: 7 and 3   [6]

Q.3) a) Compare superscalar and super pipelined   [6]

OR

b) Compare Instruction level and machine parallelism   [6]

Q.4) a) Explain Data types of 8086   [4]

OR

b) Explain any 4 Addressing modes- Immediate, Direct, Indirect, Register, Register indirect, Displacement and Stack   [4]

Q. 5) a) Explain Characteristics of memory system   [6]
b) Explain direct mapping technique with their merits and demerits.   [4]
c) Explain set associative mapping technique with their merits and demerits.   [4]

OR

Q.6) a) Explain Elements of cache design [6]

     b) Explain Performance characteristics of two level cache [4]

     c) Explain associative mapping technique with their merits and demerits. [4]

Q.7) a) Why Multicore? Explain Hardware Performance Issues [6]

     b) Explain Intel x86 Multicore Organizations [4]

     c) Explain Multicore Organization alternatives [4]

OR

Q.8) a) Why Multicore? Explain software Performance Issues [6]

     b) Explain Multicore Organization [4]

     c) Explain ARM11 MPcore processor Organizations [4]