Total No. of Questions – [08]

Total No. of Printed Pages: [02]

G.R. No.	

paper code: U228-134 (RE-FF)

May 2019/ENDSEM REEXAM

S. Y. B. TECH. (E & TC) (SEMESTER - II)

COURSE NAME: Integrated Circuits (IC)

COURSE CODE: ETUA22174

(PATTERN 2017)

Time: [**2 Hours**]

[Max. Marks: **50**]

(*) Instructions to candidates:

1) **Answer Q.1, Q.2, Q.3, Q.4, Q.5 OR Q.6, Q.7 OR Q.8**
2) **Figures to the right indicate full marks.**
3) **Use of scientific calculator is allowed**
4) **Use suitable data wherever required**

Q1 **a)** Draw neat block diagram of op-amp and describe each block in detail. **[6]**

OR

b) The following specifications are given for dual input balanced output differential amplifier at room temperature : I_E = 2.25 mA, Rc = 520 ohms, $\beta_{ac} = \beta_{dc}$ = 100, Determine i) Differential voltage gain ii) input resistance and iii) output resistance **[6]**

Q2 **a)** Draw the circuit diagram of three op-amp instrumentation amplifier and derive the expression for the gain. **[6]**

OR

b) For practical integrator the component values are R_1 =120 K ohm, R_f = 1.2 M ohm and capacitor C_f = 10 nano-farad. **[6]**

1. draw the circuit diagram
2. determine the integration frequency, f_b
3. Determine the dc gain

Q3 **a)** What is Schmitt trigger? Draw circuit of inverting Schmitt trigger and describe its working with waveforms. **[6]**

OR

b) Draw the circuit for inverting comparator. Draw the input and output waveforms with Vref = -1 V and $V_{in} = 4sin(2\pi 100t)$. Draw the transfer characteristics. **[6]**

Q4 **a)** Draw circuit diagram of first order butterworth low pass filter and describe its frequency response with the help of gain **[4]**

equation.

OR

b) Determine the cut off frequency of second order Butterworth high pass filter if R = 1 k ohm and C = 0.1 micro farad. Determine the gain of circuit at 1.59 KHz and 1 KHz. **[4]**

Q5 a) Draw the circuit diagram of R – 2R ladder type DAC. Describe how the circuit converts the code $(1\ 1)_2$ to 3/4 volts. Also draw the transfer characteristics **[6]**

b) What is the resolution of D to A converter? An 8 bit DAC has reference voltage/ full scale voltage 2.55 V. Determine its resolution/step size. **[4]**

c) Draw the circuit diagram of grounded load V to I converter and describe its operation. **[4]**

OR

Q6 a) Draw the schematic diagram of 3 bit Successive Approximation (SAR) type ADC. Describe how the circuit works and explain how it gives binary code $(1\ 0\ 1)_2$ for analog input 5.2 V. Consider analog input range between 0 to 8 V. **[6]**

b) Draw the circuit diagram of high sensitivity I to V converter and describe its operation. **[4]**

c) In a 3 bit A to D converter which accepts input voltage between 0 to 2 V, determine output voltage equivalent to 1 LSB/resolution. Vref/Full scale voltage is 2 V. What is the code that the ADC will produce for the input voltage 1.5? **[4]**

Q7 a) Describe the working of PLL with respect to the block diagram. State any three applications of PLL. **[6]**

b) In PLL IC 565 determine free running frequency, lock range and capture range. Given demodulation capacitor C= 1 micro Farad, Resistor and capacitor of VCO, R_1 = 15 k ohms and C_1 = 0.01 micro farad. Vcc = 12 V and –Vcc = 0 V (gnd). **[4]**

c) Give any two parameters of PLL and describe them with respect to transfer characteristics of PLL. **[4]**

OR

Q8 a) Draw the transfer characteristics of PLL and describe its working with its different modes of operation. **[6]**

b) Describe how PLL is used as frequency multiplier? **[4]**

c) In PLL IC 565 determine free running frequency, lock range and capture range. Given demodulation capacitor C = 2 micro Farad, Resistor and capacitor of VCO, R_1 = 12 k ohms and C_1 = 250 pico farad. Vcc = 6 V and –Vcc = - 6 V. **[4]**