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Total No. of Questions – [8]

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May 2019/ENDSEM RE-EXAM

S. Y. B. TECH. (E & TC) (SEMESTER - II)

COURSE NAME: Integrated Circuits (IC)

COURSE CODE: ETUA22174

(PATTERN 2017)

Time: [**2 Hours**] [Max. Marks: **50**]

(*) Instructions to candidates:

1) **Answer Q.1, Q.2, Q.3, Q.4, Q.5 OR Q.6, Q.7 OR Q.8**
2) **Figures to the right indicate full marks.**
3) **Use of scientific calculator is allowed**
4) **Use suitable data wherever required**

Q1 a) Define following parameters of operational amplifier along with their expressions. Also mention their ideal values. **[6]**

a) input offset voltage
b) slew rate
c) common mode rejection ratio

OR

b) Draw the circuit diagram of Widlar current source. What will be the 3-dB bandwidth of op-amp with open loop gain 10^5 and UGB of 1MHz? If the gain of the opamp is reduced to 1/1000 times of its open loop gain what will be the new BW? **[6]**

Q2 a) Why basic differentiator is needed to be modified? Draw the circuit diagram of practical differentiator along with frequency response and explain its operation. **[6]**

OR

b) Design a summing amplifier to implement $V_0 = -(3V_1+4V_2+5V_3)$. Assume R_f =100 K ohms **[6]**

Q3 a) Draw circuit diagram of triangular waveform generator and describe its working with neat waveforms. **[6]**

OR

b) Design a Scmitt trigger with UTP = 5 V and LTP = -5 V. Assume ±Vsat = ±10V. Modify the circuit to obtain UTP = 7V and LTP = - 3 V. Draw the modified circuit and waveforms. **[6]**

Q4 a) Draw circuit diagram of first order Butterworth high pass filter and describe its frequency response with the help of gain **[4]**

equation.

OR

b) What is order of filter? How it affects the frequency response of the filter. What will be the roll off rate of LPF if the order of the filter is made 5? **[4]**

Q5 a) Draw the circuit diagram of R – 2R ladder type DAC. Describe how the circuit converts the code $(0\ 1)_2$ to 1/4 volts. Also draw the transfer characteristics **[6]**

b) In a 3 bit A to D converter which accepts input voltage between 0 to 1 V, determine output voltage equivalent to 1LSB. Full scale voltage is 1 V. What is the code that the ADC will produce for the input voltage 0.75? **[4]**

c) Compare Flash ADC with Successive approximation type ADC (two points). How many comparators are needed in Flash type ADC for getting output as 4 bit code? **[4]**

OR

Q6 a) Draw the circuit diagram of 3 bit parallel comparator type/ Flash ADC to convert analog voltage in the range of 0 V to 1 V to 3 bit binary code and describe its working/operation **[6]**

b) State any two parameters of ADC. An 8 bit SAR type ADC is driven by a clock of 2MHz. Determine the conversion time required. **[4]**

c) Draw the circuit diagram of grounded load V to I converter and describe its operation. **[4]**

Q7 a) Draw the transfer characteristics of PLL and describe its working with its different modes of operation. **[6]**

b) In PLL IC 565 determine free running frequency, lock range and capture range. Given demodulation capacitor C= 2 micro Farad, Resistor and capacitor of VCO, R_1= 12 k ohms and C_1= 250 pico farad. Vcc= 6 V and –Vcc = - 6 V. **[4]**

c) What is phase detector in PLL? Describe how X-OR can be used as a phase detector. Draw its transfer characteristics. **[4]**

OR

Q8 a) What is PLL? Describe the working of PLL wrt the block diagram. State any 4 applications of PLL. **[6]**

b) In PLL IC 565 determine free running frequency, lock range and capture range. Given demodulation capacitor C= 1 micro Farad, Resistor and capacitor of VCO, R_1= 15 k ohms and C_1= 0.01 micro farad. Vcc= 12 V and –Vcc = 0 V (gnd) **[4]**

c) Describe how PLL is used as AM detector? **[4]**