Total No. of Questions – [08] Total No. of Printed Pages [02]

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MAY 2019/ENDSEM REEXAM

S. Y. B. TECH. (IT) (SEMESTER - II)

COURSE NAME: COMPUTER ORGANIZATION & MICROPROCESSOR

COURSE CODE: ITUA22175

(PATTERN 2017)

Time: [**2 Hours**] [Max. Marks: **50**]

(*) Instructions to candidates:

1) **Answer Q.1, Q.2, Q.3, Q.4, Q.5 OR Q.6, Q.7 OR Q.8**
2) **Figures to the right indicate full marks.**
3) **Use of scientific calculator is allowed**
4) **Use suitable data wherever required**

Q.1) a) Discuss the computer evolution in detail. [6]

OR

b) Explain the structure of IAS Computer with the help of diagram. [6]

Q. 2) a) Solve the following Multiplication using Booth's Algorithm. Multiplicand = 7m Multiplier =3 [6]

OR

b) Draw flow chart of Booth's algorithm for Two's Complement Multiplication. [6]

Q.3) a) Draw and explain the Control Unit Organization. [6]

OR

b) What is the role of component sequencing logic in functioning of Microprogrammed Control Unit also locate it in control unit organization. [6]

Q.4) a) Write a pseudocode for display 2-digit array elements si-> (11,22,33,44) using 8086 instructi set. Specify your assumptions clearly along with the location where result location? [4]

OR

b) Write a pseudocode for 1-digit accepts by near procedure, using 8086 instruction set. Specify your assumptions clearly along with the location where the result will get stored? [4]

Q. 5) a) Discuss cache memory and RAM in detail. Diagrammatically represent storage structure of both. [6]

b) What can the issues in cache write policy? List out the solutions for it. [4]

c) Which one is the more efficient mapping function between cache and main memory? Justify your answer. [4]

OR

Q.6) a) Draw and explain communication between CPU and main memory through 3-level cache. Also compare the performance of each component. [6]

b) Explain the impact one of the cache design parameter -block size on processor performance a list out other cache design parameters. [4]

c) Explain how the words in cache are mapped with contents in main memory with the help of Cache/Main Memory Structure [4]

Q.7) a) Diagrammatically represent the alternative chip organizations available for. [6]
i) Superscalar ii)Simultaneous multithreading iii) Multicore

b) Compare simple procedure oriented approach with simultaneous Multithreading approach. [4]

c) What are the software performance issue, discuss in brief. [4]

OR

Q.8) a) What is Multicore? Explain any one multicore organization. [6]

b) What are different techniques for parallel processing? Explain any one in brief. [4]

c) What is the role of Multicore in improving the performance? Brief about working of any on real-time applications for the same. [4]