Total No. of Questions – [03]

G.R. No.

Total No. of Printed Pages: 01
Paper code U239-141 (T1) IT.
U239-121 (T1) comp.

OCTOBER 2019/ INSEM (T1)
S. Y. B.TECH. (COMPUTER ENGINEERING/INFORMATION TECHNOLOGY)
(SEMESTER – III)
COURSE NAME: ANALOG AND DIGITAL ELECTRONICS
COURSE CODE: CSUA21181/ITUA21181
(PATTERN 2018)
(Model Answer)

Time: [1 Hour]   [Max. Marks: 20]

Q 1 a) Definition of 1's & 2's complement should be written with one example each
[4 marks].
Map the given SOP expression into K-map and do the grouping of cells [2 marks]
Obtain minimized expression and design logical circuit diagram   [2 marks]

Q 1 b) Draw minimized table (expected 3 tables)   [2 marks]
Find minimized expression   [1 mark]
Find PI and EPI from the table   [1 mark]

Q 2 a) Design Truth Table for conversion   [2 marks]
Obtain SOP expression   [2 marks]
Map SOP expression into K-Map   [2 marks]
Draw Logical Circuit Diagram   [2 marks]

Q.2 b) Draw block diagram of BCD adder with explanation   [2 marks]
Describe three cases with examples   [6 marks]

Q. 3 a) Draw J-K Flip-Flops block diagram   [1 mark]
Truth Table   [1.5 marks]
Excitation Table   [1.5 marks]

Q.3 b) Draw Truth Table of S-R flip flop   [2 marks]
Draw block diagram for conversion of S-R Flip Flop to J-K Flip Flop   [2 marks]