October 2019 / INSEM (T1)

S.Y. BTECH (PROGRAM) (SEMESTER-I)

Paper code - U239-144 (T1)

Course name : Computer organization.

Course code : ITUA 21184

(pattern 2018)

Time : 1 hr Total marks: [2

Q.1

a) IAS (Von Neumann architecture [Total 8 mks

i) Diagram ——— [2]

ii) Explanation ——— [2]

iii) Main memory & I/O devices – [2]

iv) CPU components ——— [2]
(IAS details)

b) Computer components ——— [Total 8 mks].

i) CPU components (With all registers) – [2]

ii) I/O modules ——— [2]

iii) System Bus ——— [2]

iv) Main memory ——— [2]

Q.2

a) Multiply –7 x –3 using booth's algorithm.
Register size = 4.

⇒ Multiplicand → $(-7)_{10}$ → $(1001)_2$

Calculate –M ⇒ $(0111)_2$

1001

0110 (1's complement

+ 1

0111

$Q = (-3)_{10} = (1101)_2$

	AC	Q	Q_{-1}	operation.
cycle ①	0000	1101	0	i) AC ← AC − M 0000 + 0111 0111 ii) A.S.R.
	0111 → 0011	1101 → 1110	0 → 1	
cycle ②	1100	1110	0	i) AC ← AC + M. 0011 + 1001 1100. ii) A.S.R.
	1110 → 0111	1110 → 0111	0 → 0	
cycle ③	0101	0111	0	i) AC ← AC − M 1110 + 0111 1 0101 Discard carry. ii) A.S.R.
	0010	1011	1	
cycle ④	0001	0101	1	i) A.S.R.

Now Ans: $(00010101)_2 = (21)_{10}$.

So $(-7)_{10} \times (-3)_{10} = (21)_{10}$.

1.3 (ab)

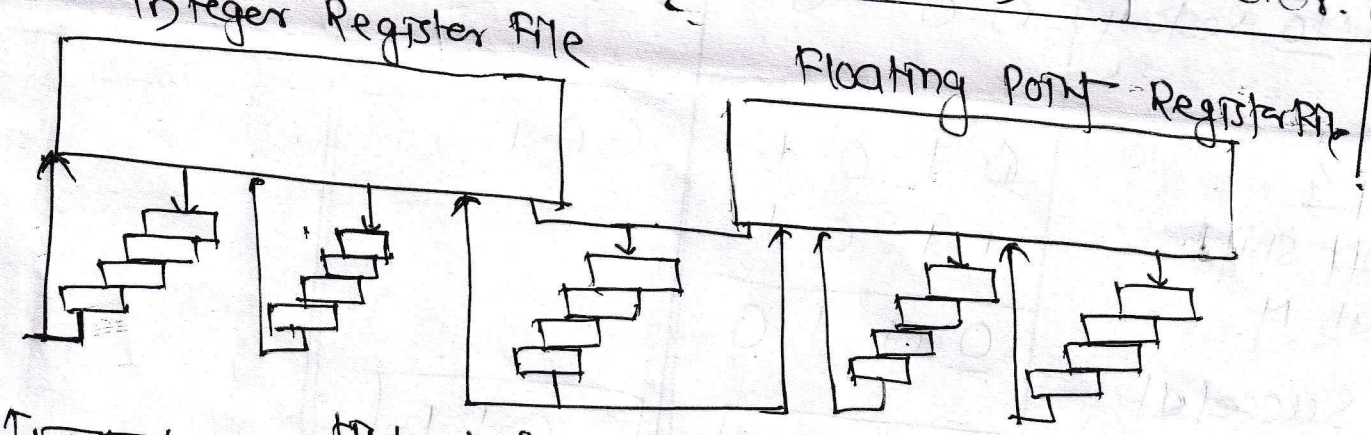
11 → +11 → 1011, -11 → 0101

3 → +3 0011, -3 1101

	Accumulator (A)	Divident (Q) (11)	Divisor (M) (3)
	0000	1011	0011
Step 1: left shift ← Sub M (-3) ∴ Unsuccessful ∴ Restore & 0	0001 +1101 1110 0001	011_ 0110	
Step 2: Left shift Sub M Unsuccessful ∴ Restory value	0010 1101 1111 0010	110_ 1100	
Step 3 left shift Sub M Successful ∴ No Restory	0101 1101 0010 0010	100 1001	
Step 4 left shift Sub M ∴ Successful ∴ No Restory.	0101 1101 0010 0010	001 0011	
	Remainder → 02	Q → 03	

Differentiate between superscalar and super pipelined

Super scalar	Super Pipelined
1. Dividing the long latency stages of a pipeline into several shorter stages.	1. Dynamically issuing, Executing Multiple Instruction per cycle
2. Superscalar seeks to improve the parallel instruction rate.	2. Super-pipelining seeks to improve the sequential instruction rate.
3. Superscalar perform only one pipeline stage per clock cycle in each parallel pipeline.	3. Super-pipeline system is capable of performing two pipeline stages per clock cycle.
4. Superscalar complex to design	4. Super pipelined relatively easy than superscalar.



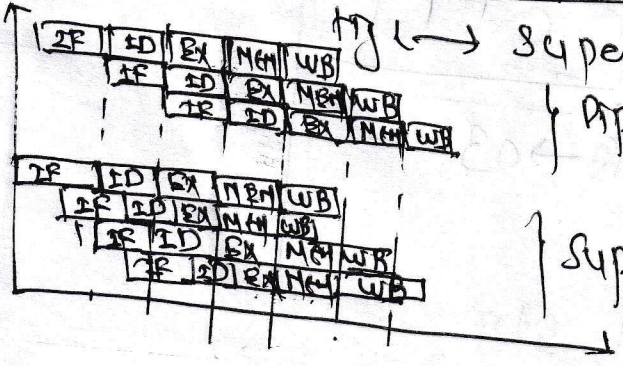
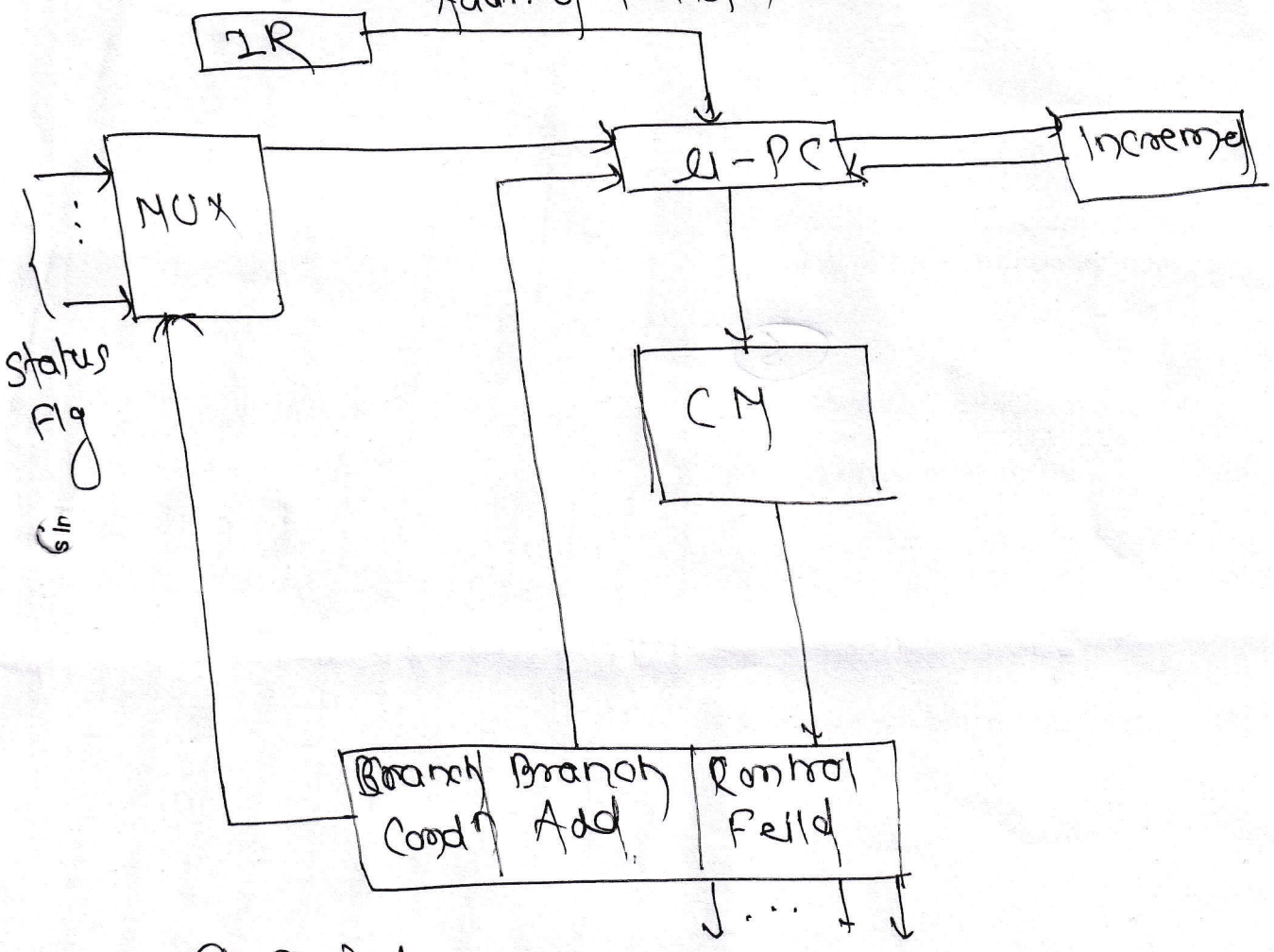


fig → superscalar, organization.

Microprogram – Micro Instruction

* Program is set of instructions.
- An instruction required a set of small operations called Micro-operations.
- Micro-operation needs control signal to execute and for control signal we need set of micro instruction, we called micro-program – micro instruction.



Adv : ① Flexible
② Scalable

Dis : ① Cost is High