Total No. of Questions – [06] Total No. of Printed Pages: 02

G.R. No.	

DECEMBER 2021 - ENDSEM EXAM
S. Y. B. TECH. (E&TC) (SEMESTER - I)
COURSE NAME: Digital System Design
COURSE CODE: ETUA21204
(PATTERN 2020)

Time: [1 Hour] [Max. Marks: 30]

(*) Instructions to candidates:

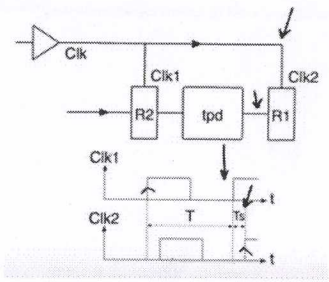
1) **Answer Q.1 OR Q.2, Q.3 OR Q.4, Q.5 OR Q.6.**
2) **Figures to the right indicate full marks.**
3) **Use of scientific calculator is allowed**
4) **Use suitable data where ever required**

Q.1) a) Show how an asynchronous counter with D flip-flops can be implemented having a modulus of thirteen with a straight binary sequence from 0000 through 1100. Draw the timing diagram for the same. [4]

b) Construct a synchronous decade counter using JK flip-flops. Use k-map for design. Draw the timing diagram for the same. [6]

OR

Q.2) a) Compute the minimum required clock period if t_{su} = 1 ns, t_{CQ} = 1 us, t_{pd} = 2 us, and T_s = 0.5 us and determine the maximum frequency of operation. [4]



b) Build a counter to produce the following binary sequence. Use J-K flip-flops. [6]
1, 4, 3, 5, 7, 6, 2, 1

Q.3) a) Construct a CMOS circuit for $Y = \overline{(A+B).(C+D)}$ [4]

b) Build a 2 input TTL inverter and verify the truth table of it from your design. [6]

OR

Q.4) a) "CMOS logic family is superior than bipolar families," Justify. [4]

b) Using PAL realize the following expressions: [6]
F_1 (A, B, C) = ∑m (0, 3, 4, 7) and F_2 (A, B, C) = ∑m (0, 2, 4)
Optimize expressions using k-map before implementation.

Q.5) a) Evaluate the output of the following operators. [4]
i) "1100" srl 2, ii) "1100" sra 2, iii) "1010" ror 1, and iv) "1010" sll 1

b) Design BCD to seven-segment LED decoder for common-anode display using VHDL. [6]

OR

Q.6) a) Design a 1-bit full adder using structural style of modelling. [4]

b) Design 4-bit up/down counter using VHDL. If the MODE input is '0' it should count in the up mode and if '1' it should count in down mode. Use RESET input to reset the counter. [6]