G.R. No.	

DECEMBER 2021 - ENDSEM EXAM
S. Y.B. TECH. (INFORMATION TECHNOLOGY) (SEMESTER I)
COURSE NAME: COMPUTER ORGANIZATION
COURSE CODE: ITUA21205
(PATTERN 2020)

[Max. Marks: 30]

Time: [1 Hour]

Instructions to candidates:
1) Answer Q.1 OR Q.2, Q.3 OR Q.4, Q.5 OR Q.6.
2) Figures to the right indicate full marks.
3) Use of scientific calculator is allowed
4) Use suitable data where ever required

Q.1 a) Explain Immediate addressing and direct addressing mode with example [4]
b) Summarize register organization of 8086 Processor [6]

OR

Q.2 a) Explain indirect addressing mode and Register addressing mode with example. [4]
b) Construct an instruction pipeline & show how it will increase the performance of processor. [6]

Q.3 a) Categorize the cache memory into different level & illustrate the use of each level. [4]
b) Compare the uses of memory hierarchy in a computer system by using a suitable diagram [6]

OR

Q.4 a) Distinguish between one level and two-level cache. [4]
b) Consider a reference string: 4, 7, 6, 1, 7, 6, 1, 2, 7, 2. the number of frames in the memory is 3. Evaluate the number of page faults respective to: FIFO Page replacement algorithm [6]

Q.5 a) Give several reasons for the choice by designers to transfer to a multicore organization rather than increase parallelism within a single processor [4]
b) Compare the differences among single core Architecture & Multicore Organizations? Describe Recent trends in Multicore. [6]

OR

Q.6 a) Sketch & Explain multiprocessor architecture. [4]
b) Categorize the hardware and software performance issues of multicore architecture [6]