MARKING SCHEME

May 2022 (ENDSEM) EXAM

T.Y. B. TECH. (SEMESTER - II)

COURSE NAME: Digital System Design using Verilog

COURSE CODE: ETUA32182C

(PATTERN 2018)

Q.1	**a)** architecture of XC9572 CPLD and Explanation each block in brief. **b)** Optimization of equations Construction of optimized combinational circuit using PLA. **OR** **b)** Optimization of equations Construction of optimized square look-up table for decimal numbers 0 to 5 using ROM.	[2 marks] [2 marks] [2 marks] [4 marks] [2 marks] [4 marks]
Q.2	**a)** Correct diagram Verilog code to design 2kB RAM with a word size of 8 bit with separate read/write data bus. **b)** State diagram of sequence detector to detect an overlapping sequence "1101" using Mealy FSM. Verilog code. **OR** **b)** State diagram to construct a serial adder. Verilog code.	[2 marks] [2 marks] [3 marks] [3 marks] [3 marks] [3 marks]
Q.3	**a)** List of micro-operations for the pipelined stage Instruction Fetch (IF). Stage diagram to implement these micro-operations. **b)** Pipelined architecture. Verilog code to implement this architecture. **OR** **b)** Complete instruction subset being considered for the MIPS32 processor design.	[2 marks] [2 marks] [3 marks] [3 marks] [6 marks]