Total No. of Questions – [3] Total No. of Printed Pages: 02

G.R. No.	

PAPER CODE	U321-242C(ESE)

May 2022 (ENDSEM) EXAM

T.Y. B. TECH. (SEMESTER - II)

COURSE NAME: Digital System Design using Verilog

COURSE CODE: ETUA32182C

(PATTERN 2018)

Time: [1Hr] [Max. Marks: 30]

(*) Instructions to candidates:

1) **Figures to the right indicate full marks.**
2) **Use of scientific calculator is allowed**
3) **Use suitable data where ever required**

Q.1 **a)** Draw architecture of XC9572 CPLD and comment on each block in brief. **[4]**

b) Construct an optimized combinational circuit for the given truth table using PLA. **[6]**

Inputs			Outputs	
A	B	C	F1	F2
0	0	0	1	1
0	0	1	1	0
0	1	0	1	0
0	1	1	0	0
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	0	1

OR

b) Construct optimized square look-up table for decimal numbers 0 to 5 using ROM. **[6]**

Q.2 **a)** Write a Verilog code to design 2kB RAM with a word size of 8 bit with separate read/write data bus. **[4]**

b) Construct a sequence detector to detect an overlapping sequence "1101" using Mealy FSM. Draw state diagram and write a Verilog code. **[6]**

OR

b) Construct a serial adder in Verilog using FSM. Draw state diagram. **[6]**

Q.3 **a)** List the micro-operations for the pipelined stage Instruction Fetch (IF). Draw the stage diagram to implement these micro-operations. **[4]**

b) Construct the pipelined architecture to do the following computations. Write a Verilog code to implement this architecture. **[6]**

x1 = A + B; x2 = C – D; x3 = x1 + x2; F = x3 * D;

OR

b) List the instruction subset being considered for the MIPS32 processor design taught in the lectures. **[6]**